Real Time CMOS Optical Processor for a Shack Hartmann Wavefront Sensor

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Abstract

A real time VLSI optical centroid processor has been developed as part of a larger Shack-Hartmann wavefront sensor system for applications in adaptive optics. The implementation of the optical centroid detection system was demonstrated successfully using a hardware emulation system. Subsequently, the design has been implemented as a CMOS single-chip solution. This has advantages in terms of power consumption, system size and cost. The design of the different components of the system will be discussed along with test results of the fabricated device.

Keywords

Special Issue Sensors 2002, centroid detection, wavefront sensor, photodiodes, active pixel, FPGA, CMOS IC, integrated detector

INTRODUCTION

For imaging or video applications, CCDs (charge-coupled devices) are the preferred technology because of their high-quality images [1]. However, for machine vision or sensor applications where the output does not consist of images but of extracted, interpreted data, CMOS offers the advantages of random access to pixel regions of interest, low power dissipation and high level of integration. This additional integration provides on chip local processing thus allowing enhanced performance and a reduction in overall system cost. Our intended application is that of an integrated CMOS Shack Hartmann wavefront sensor for an adaptive optical system.

APPLICATIONS AND WORK DONE

Aberration caused by the turbulence in the atmosphere can degrade the imaging property of the light being detected by distorting the incoming wavefront. A Shack-Hartmann wavefront sensor [2] uses an array of small lenslets to sample the optical wavefront (Figure 1). Local wavefront tilts are measured by detecting the deviation of the focussed spots from reference positions. Traditional systems use a single CCD to sample the entire wavefront resulting in a data bottleneck. In our system, each local wavefront tilt is measured by a local tilt sensor with its own detector array and local centroid processing. The array of tilt sensors will be linked to a matrix processor to reconstruct the estimate of the complete wavefront. Once calculated, the reduced bandwidth wavefront data can then be transferred off-chip. Hence, parallel processing is achieved whereby the data rate is independent of the number of tilt sensors employed.

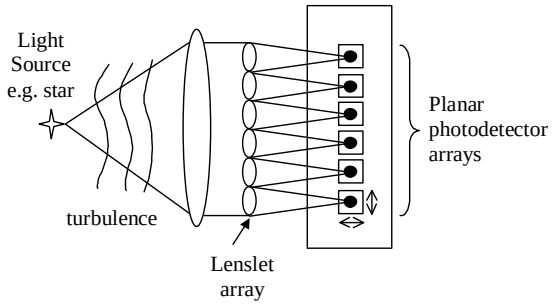

Figure 1. A Shack Hartmann wavefront sensor

Centroiding Systems

There are several types of optical front-end devices besides CCDs that can be used in a centroiding or position sensing system, namely lateral-effect photodiodes (LEP) or position sensitive detectors (PSD); quad cells or quadrant detectors; and multi-pixel arrays. Conventional LEPs have high linearity but require a very uniform resistive layer with large sheet resistance, which is not generally available with a standard CMOS process. Quad cells have simple readout schemes but are not very linear. They are designed primarily for measuring small deviations because the incident beam must impinge simultaneously on all four sectors of the detector. With sufficient number of pixels,

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multi-pixel array systems have very high linearity and good sub-pixel accuracy but require complex readout and processing schemes.

From a processing point of view, there are several methods of computing the centroid of a light spot. Most LEP systems [3] have the processing performed off-chip because the LEP itself is not fabricated on a standard CMOS process, and because of its simplicity, the processing tends to be implemented in analogue. Computation of quad cell systems [4] is also usually performed in analogue. Most multi-pixel array systems [5,6,7,8] use an analogue current dividing method to find the centroid which require the use of a linear resistive or capacitive array. Using analogue centroid computation offers the advantage of high speed and high functional density. However, they suffer from mismatch and poor tolerance of the polysilicon resistors or capacitors in the divider line. Also, as CMOS technology scales, the advantages of speed and functional density of analogue over digital diminishes. A generic 256 x 256 pixel array system with an on-chip image processor has been designed which performs several common image-processing algorithms including centroiding [9]. However, in an adaptive optics system such as the Shack Hartmann wavefront sensor, a large number of tilt sensors are required but the pixel count of each tilt sensor can be minimal. The design, simulation and layout of a 5 x 5 tilt sensor for just such a system will be presented in this paper.

Hardware Emulation System

Initially a hardware emulation system [10] was designed. This allowed us to test the optical processing and system control algorithms prior to CMOS foundry fabrication. The system consisted of a 5 x 5 photodetector array, multiplexers, a current-to-voltage converter, a single channel 16-bit analogue-to-digital converter (ADC), a Field Programmable Gate Array (FPGA) for centroid computation and an RS232 serial interface for transmitting centroid data to a PC. The system was tested using both a commercial photodiode array and our own full custom CMOS photodetector array. The centroid is computed by multiplexing each photodiode output into a current-to-voltage converter, which is then digitised by the ADC. The FPGA then computes the centroid and transmits this in RS232 format to the PC. The sampling frequency of the ADC was 40kHz and a centroid was successfully computed once every 0.75ms.

SYSTEM DESIGN

After the hardware emulator verified the performance and functionality of the system, the design was implemented in a single CMOS IC. A block diagram of the overall system is shown in Figure 2. It consists of an active pixel sensor array, the analogue front end and analogue-to-digital conversion circuitry, the digital centroid processor and a serial link for transmitting and receiving data off-chip. The individual components of the system are discussed in more detail in the following sections.

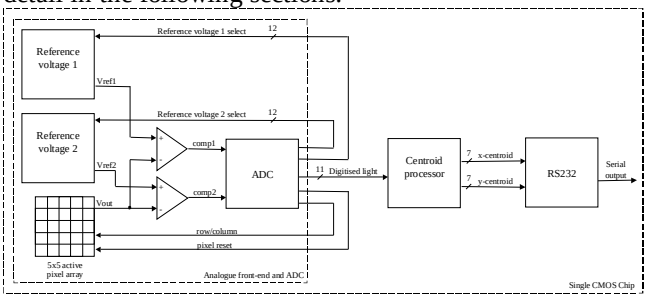
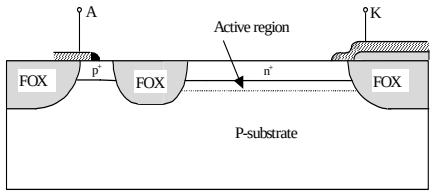


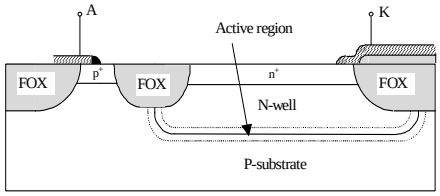
Figure 2. Block diagram of optical centroid detection system

On-chip CMOS Photodetectors and Integrating Active Pixel Sensor (APS) Array

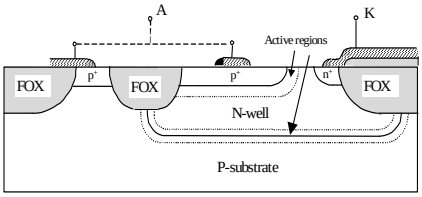
Several prototype photodiodes were previously implemented in a standard 0.7μm N-well CMOS process [10] namely: the shallow (diffusion-substrate or diffusion-well) photodiodes; the deep (N-well to p-substrate) photodiode; and the combined deep and shallow (p+ to N-well) photodiode (Figure 3). The shallow photodiodes have better spectral response at shorter wavelengths while deep photodiodes have better spectral response at longer wavelengths. The responsitivities of the photodiodes compare favourably with commercial photodiodes and is of the order of 0.4 A/W. For the photodiode array, the deep N-well to p-substrate photodiode is used as it is found to have a reverse bias current that is minimally affected by the reverse bias voltage, unlike the shallow and combined photodiodes (Figure 4). The I-V characteristics of the deep photodiode in room light and in the dark is shown in Figure 5.



(a) Shallow n+ photodiode



(b) Deep N-well photodiode



(c) Combined shallow and deep photodiodes

Figure 3. Three different photodiode configurations implemented in a standard 0.7µm CMOS process

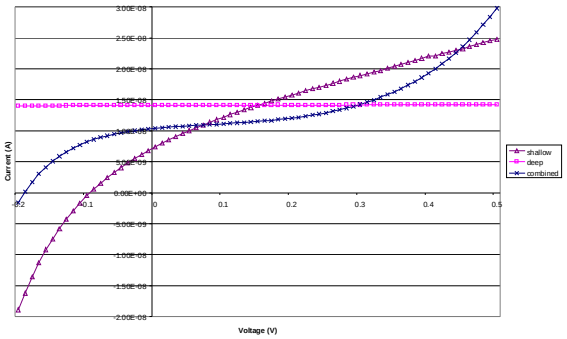
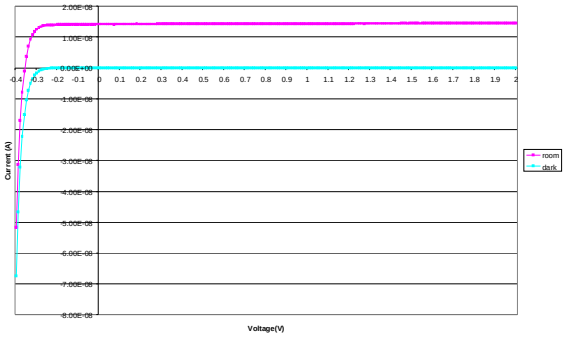
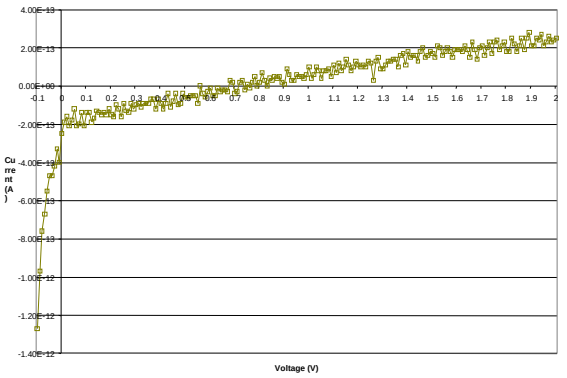


Figure 4. I-V plots of deep, shallow and combined 100µm x 100µm photodiodes in room light



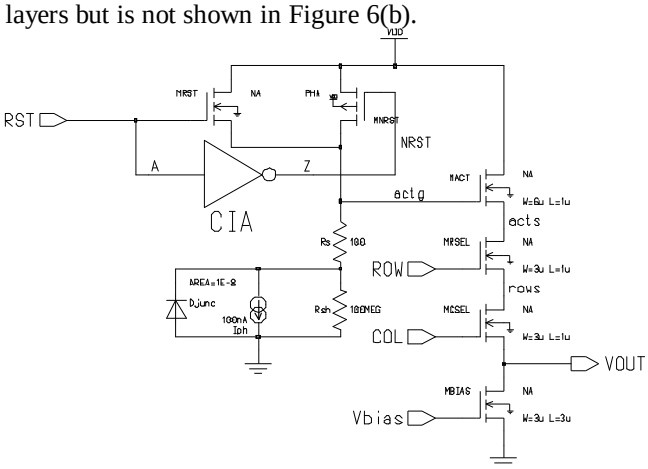
(a) In room light and in dark



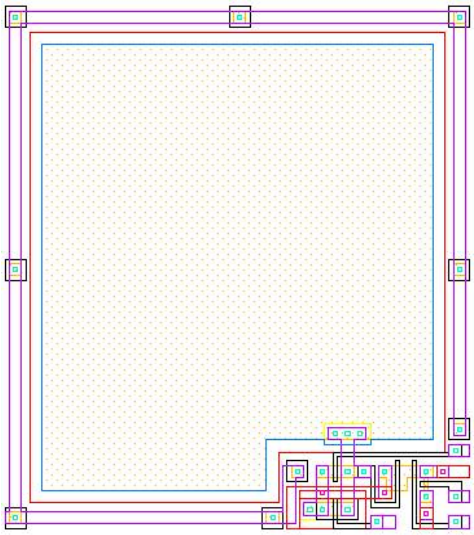
(b) Close up of dark current

Figure 5. I-V plots of deep photodiodes in room light and in dark

A 5 by 5 photodiode array is used with each pixel having a size of 100µm x 100µm. For each pixel, an integrating active pixel structure is employed and is shown in Figure 6(a). This consists of a single n-well/p-substrate photodiode, a complementary NMOS/PMOS reset gate, a source follower and row-column select transistors. All pixels are reset globally and the inverter output and the bias transistor (MBIAS) are shared with all pixels. Having a CMOS transmission gate allows the pixel to be pulled up to 5V during reset. This eliminates the problem obtained with using only an NMOS reset transistor whereby the reset level varies with light intensity. The layout of this circuit is shown in Figure 6(b). Circuitry other than the photodetector is light shielded using one of the two available metal layers but is not shown in Figure 6(b).



(a) Active pixel circuit



(b) Layout of active pixel

Figure 6. Active pixel circuit and its layout

Each pixel is globally reset to 5V for 8µs (with a 32MHz clock) after which the pixel photodiode is allowed to discharge through its own photocurrent (Figure 7). The discharge rate is proportional to the photocurrent of that pixel, which in turn is proportional to its incident light level. The discharge curve is approximately linear for voltages above 1V. This is because the photodiode capacitance varies inversely with the square root of the diode voltage. Also, as the diode and the pixel output voltage drops the bias transistor starts to operate in the linear region and is no longer independent of the output voltage. By measuring the time taken for the voltage to drop to a particular voltage level in the linear region, a reading proportional to the converted light level is obtained. The discharge time is measured by starting an 8-bit counter when it passes through an initial voltage level and stopping it when it

passes a second lower voltage level. These voltage levels are set by reference voltage generators. A programmable discharge clock is used such that for different discharge rates or intensity levels, optimum resolution can be maintained. Four programmable discharge clock frequencies are possible, which are internally selected by two mode registers. The states of which can be read via the on-chip RS232 receiver.

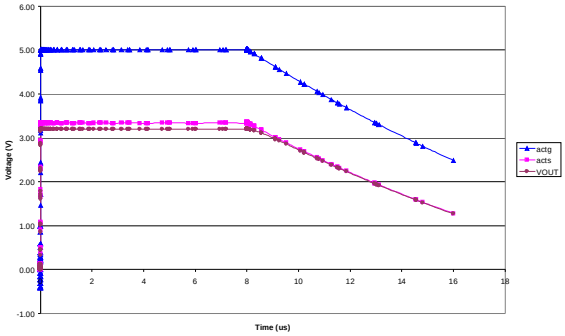


Figure 7. The discharge curve of the active pixel circuit used

The backend of the active pixel sensor in Figure 6(a) acts as a source follower buffer for the photodiode node (Figure 8). It consists of the source follower active transistor (MACT), a row select transistor (MRSEL), a column select transistor (MCSEL) and a bias transistor (MBIAS) shared by all pixels.

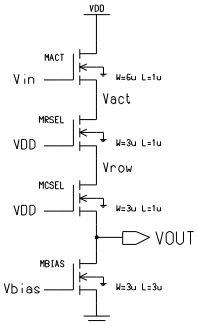


Figure 8. Backend of the active pixel sensor

Simulation and Circuit Analysis

To optimize the design of the backend, simulations were carried out to find the optimum W/L of the transistors and biasing voltage. The gates of the row-column access transistors were held at VDD i.e. 5V. The results showed that as *Vbias* or the W/L ratio of MBIAS is increased, the dynamic range is reduced and the response becomes more non-linear. Figure 9 shows the transfer functions obtained as *Vbias* is swept. An optimum bias voltage of 1V was selected to keep the biasing transistor operating above the threshold voltage of 0.76V but sufficiently small so as to maintain a wide linear operating range. For further optimisation after fabrication, the applied voltage of the bias transistor of the active pixel array can also be applied externally. Simulations also showed that increasing the W/L ratios of MACT, MRSEL, MCSEL improves the DC voltage gain and linearity of the transfer function. The selected W/L ratios of the transistors are shown in Figure 8.

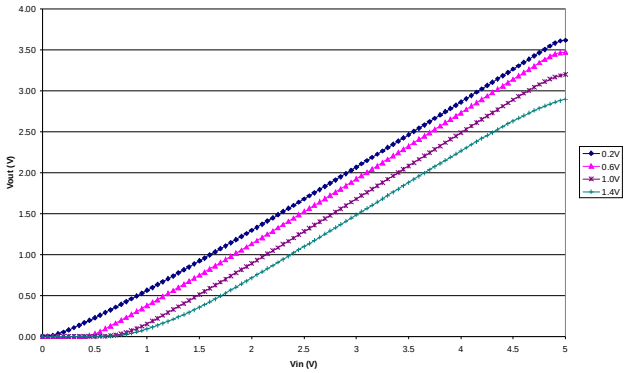


Figure 9. VOUT against Vin for different values of Vbias (W/L = 3µm/3µm)

First order circuit analysis of the circuit produces an output voltage given by:-

$$Vout = Vin - V_{T_{MACT}} - \sqrt{\frac{K_{MBIAS}}{K_{MACT}}}\left(Vbias - V_{T_{MBIAS}}\right) - \frac{K_{MBIAS}}{2K_{MRSEL}}\frac{\left(Vbias - V_{T_{MBIAS}}\right)^2}{\left(VDD - Vrow - V_{T_{MRSEL}}\right)} - \frac{K_{MBIAS}}{2K_{MCSEL}}\frac{\left(Vbias - V_{T_{MBIAS}}\right)^2}{\left(VDD - Vout - V_{T_{MCSEL}}\right)}$$

Furthermore, it shows that for small output voltages, as Vbias increases the non-linearity increases due to the last three terms in the above equation.

Analogue Front End and ADC

The analogue front-end and ADC (shown dotted on the left hand side of Figure 2) consists of the active pixel array, 2 sets of reference voltage generators, 2 comparators with its biasing and the analogue-to-digital conversion circuitry, which includes row-column decoders and counters. Each set of reference voltage generators can generate a voltage between 1V and 3.75V with a step size of 0.25V and each connects to a comparator input. Six levels of one of these reference generators are shown in Figure 10. The reference voltage generator consists of a set of voltage dividers implemented using active resistors and transmission gates for selecting the desired voltage. These transmission gates are used to select the switching points of the comparators during analogue-to-digital conversion. Using a series chain of active resistors instead of a single active resistor reduces the area required.

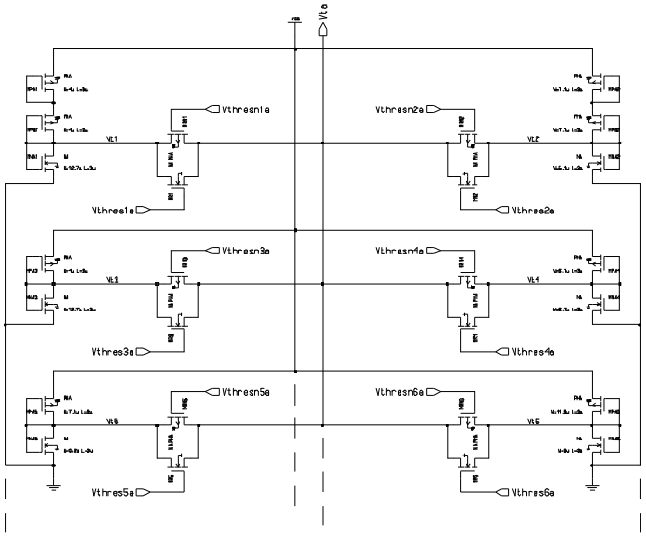


Figure 10. Reference voltage generator

When reset is fired, one reference voltage (Vref1) will be set at 3.75V while the second reference voltage (Vref2) will be set at 3.5V. Then the reference voltages are decreased until both reference voltages are below the pixel-reset level. This is determined by when the comparators switch over. In order to cope with a wide range of light levels, three modes of operation have been designed. In the first mode, the counter is started when the reset is removed and stopped when the discharge curve passes the 1st reference voltage. In the second mode, the counter is started when the discharge curve passes the 1st reference voltage and stopped when it passes the 2nd reference voltage. This has the advantage that if the reset level varies from pixel to pixel, the reading will be independent of this offset. In the third mode, a 2-cycle approach is used. In the 1st cycle, a reading is obtained as in mode 2. In the 2nd cycle the value of Vref2 is adjusted such that a larger dynamic range is obtained thereby increasing the resolution for higher light levels.

Digital Backend

The digitized light level at each pixel is then fed into the centroid processor - previously demonstrated with the FPGA hardware emulation system [10]. The centroid is found from the calculation of the first order moment of the intensity distribution of the array. This requires the multiplication of the intensity of every pixel with the weighting of its position. The summation of which is divided by the overall sum of the intensities of every pixel to give the 7-bit x and y centroids (Figure 11).

The centroid of an array of photo-detectors is expressed in terms of its x and y coordinates, C(x) and C(y). The values of C(x) and C(y) and hence the centroid of the array are found from the "1st moment" equations:

$$C(x) = \frac{\sum r_{xn} I_n}{\sum I_n}; \qquad C(y) = \frac{\sum r_{yn} I_n}{\sum I_n};$$

where r_{xn} is the displacement in the x-direction

r_{yn} is the displacement in the y-direction

I_n is the light (current) level of each photodetector

The processor also determines the maximum light level and the position of the pixel with the maximum light level (not shown in Figure 11).

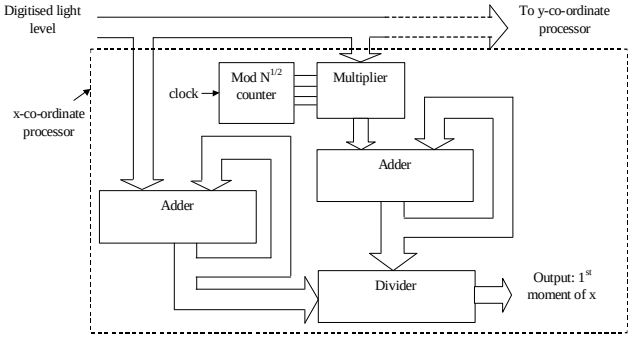


Figure 11. Block diagram of centroid processor in the x-direction

These values are then transmitted off-chip serially using the RS-232 format. For testing purposes, the x-dividend, y-dividend, divisor and the individual pixel light level can also be transmitted off-chip. With this design, a centroid value is output once every frame and a frame lasts 26 pixel periods i.e. a frame rate of between 2.4kHz and 4.8kHz depending on the incident light level of every pixel. This is an improvement over the hardware emulation system previously demonstrated which could output centroids at a rate of 1.3kHz. Using an adjustable baud rate of up to 115200 bits/s, the transmitted values will be observed in real-time. For observability, the reset of the pixels and the row-column addressing can also be controlled externally.

CAD TOOLS, LAYOUT AND FABRICATION

The CAD tools used were the Mentor Graphics version C4 tools running on Solaris 7 on a Sun Ultra 60 Workstation. The mixed analogue and digital CMOS 0.7μm libraries were provided by Alcatel Microelectronics (Mietec) via Europractice. The process was a double metal, single poly n-well process with a gate density of 1250/mm^2. Schematics were entered via "Design Architect". Initially, "Accusim" is required to simulate the analogue front-end. The models of transistors, diodes and the standard cells were provided by Mietec. Then the output signals of the comparators are fed into the digital circuitry for digital simulation using "QuickSim". The digital circuitry was synthesised from VHDL code into Mietec digital components using "Leonardo Spectrum". Static timing analysis includ-

ing delay path analysis and slack analysis was carried out using "QuickPath". Finally, when the design had been thoroughly simulated and its performance verified the layout was implemented using “IC station” (Figure 12). The chip contained 7200 logic gates and has a size of 4500µm x 4000µm. This will scale favourably as technology scales and as we move towards a triple metal process with improved routing capabilities. Also, because the division process is performed only once every frame, the divider, which makes up a significant amount of the processing, can be shared with several arrays without increase in size or loss of speed.

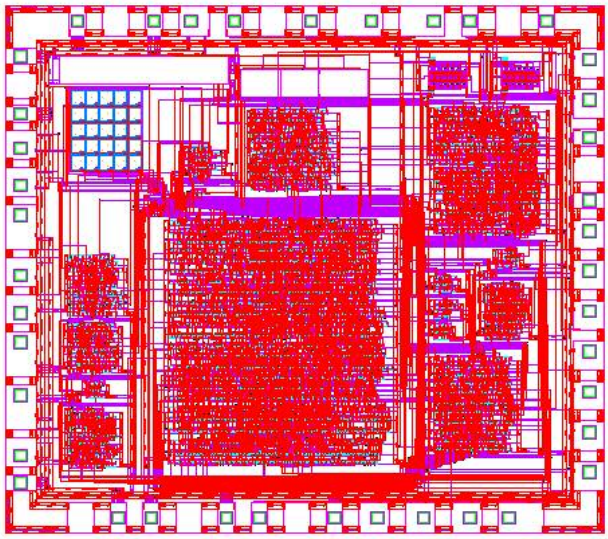


Figure 12. Layout of the tilt sensor

EXPERIMENTAL RESULTS

A 3µm diameter beam from a 633nm HeNe laser was scanned across the array at a speed of 2000µm/sec. Centroid values were computed by the processor and serially transmitted in real time to a PC. The maximum rate of generation of these centroid values was found to be 4.8kHz. Figures 13 and 15 show grey scale maps of the x and y-centroid values successfully recorded at each position on the array. The dark regions correspond to smaller centroid coordinates whilst lighter regions correspond to larger centroid coordinates. As expected, as we scan in the x-direction, the x-centroid values increases while the y-centroid values remain constant and vice versa. Since the laser beam size is less than the size of one pixel, a stepped appearance can be seen as the beam moves across the array passing from one discrete detector to another. Figures 14 and 16 show the x and y-centroid values plotted as a function of pixel position.

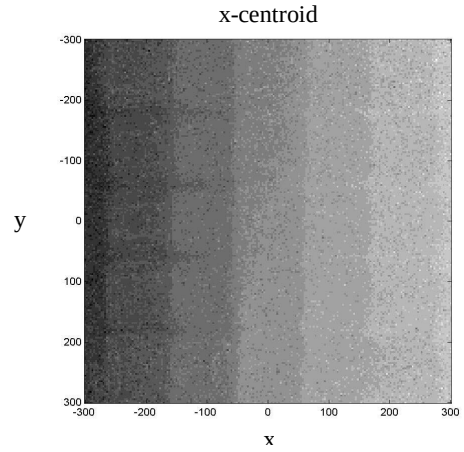


Figure 13. Image map of x-centroids

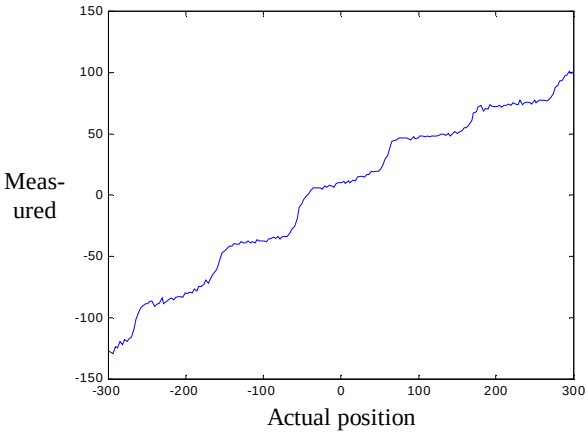


Figure 14. Measured vs. actual position of x-centroids

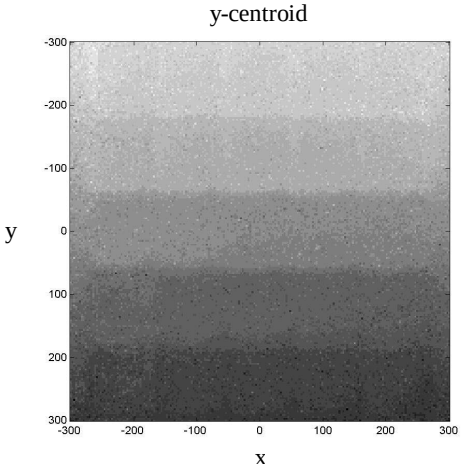


Figure 15. Image map of y-centroids

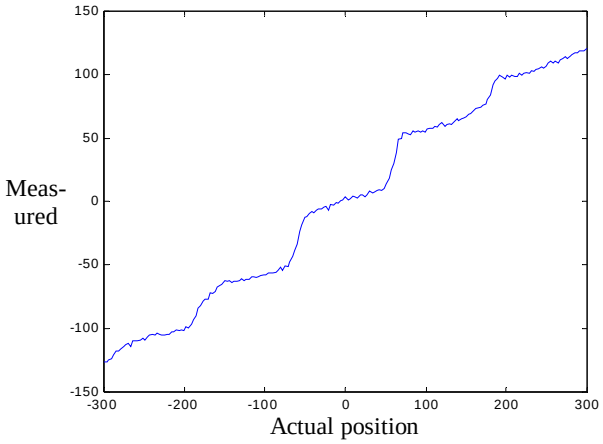


Figure 16. Measured vs. actual position of y-centroids

CONCLUSIONS

A real time VLSI optical centroid processor was successfully designed and fabricated for integration into a proposed Shack-Hartmann wavefront sensor. The chip consists of an optimised 5 x 5 active pixel array and analogue-to-digital conversion circuitry integrated with the centroid processor previously demonstrated using a hardware emulation system. Centroid values can be outputted at a rate of more than 2.4kHz allowing real time performance of the adaptive optical system.

ACKNOWLEDGMENTS

The authors are grateful for the financial support of the University of Nottingham, University of Nottingham International Office, University of Nottingham in Malaysia and the Engineering and Physical Sciences Research Council (EPSRC), UK.

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