The Design and Characterisation of an Optical VLSI Processor for Real Time Centroid Detection

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ABSTRACT

The integration of photo-detectors onto a standard CMOS integrated circuit is presented. This device provides the optical front end for a real time centroid detection system to be used as part of a larger system for implementing a Shack-Hartmann wavefront sensor. A hardware emulation system containing a Field Programmable Gate Array is used to prototype suitable algorithms prior to IC fabrication. Data is presented on the performance of photodetectors and the ability to extract in real time a centroid coordinate.

Keywords: centroid detection, wavefront sensor, photodiodes, active pixel, FPGA, CMOS IC, integrated detector

1. INTRODUCTION

The fabrication of photodetectors integrated with complex analogue and digital circuitry on a single integrated circuit presents numerous applications and opportunities to the optical design engineer. Such integration provides potential for improvement in speed, cost and performance over traditional systems. These traditional systems require data to be transmitted from the optical sensor (i.e. a CCD) to a host computer by means of an analogue video line, an analogue-to-digital converter (ADC) and a frame memory and hence are invariably slow and costly. A CMOS sensor on the other hand allows random access to pixel regions of interest. This readout facilitates windowed and scanning readouts that can increase the frame rate at the expense of reduced resolution. The strength of CMOS as compared to CCD technology is not in sensor cost itself, but in the higher level of integration offered by CMOS, which allows a reduction in the number of external chips used in the system and therefore a reduction in overall system cost. This additional on chip processing thus offers potential for enhanced performance for the chosen application. A CCD imaging system is more suited to high-resolution or colour imaging where cost is less important but image quality is paramount. With its large frame sizes/pixel count, CCDs are not able to achieve frame rates in the high kilohertz or megahertz range and hence are not able to operate in real time for systems requiring such high frame rates. As a result many applications would benefit from a simplification of the CCD system.

Three factors have influenced the arrival of these devices. Firstly, in the early 1990's a demand existed from the high street market for a range of image sensors where the quality was not of importance but the size and price was paramount. Secondly, space agencies (i.e. NASA and ESA) required an extremely low power image sensor with combined low component count but without compromising the quality. This resulted in significant advances in CMOS image sensors and the development of the CMOS active pixel sensor (APS). Thirdly, over these past ten years CMOS technology in general has advanced faithfully following Moore's law.

The integrated CMOS optical processor is thus an extremely powerful device that has yet to be fully utilised by the optical design engineer. Although a plethora of applications exist the specific application that this paper addresses is the centroid detection of incoming light to be used as a wavefront sensor.

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2. CENTROID DETECTION

Aberration caused by the turbulence in the atmosphere can degrade the imaging property of the light being detected by distorting the incoming wavefront. A Shack-Hartmann wavefront sensor[1] uses an array of small lenslets to sample the optical wavefront. Local wavefront tilts are measured by detecting the deviation of the focussed spots from reference positions. These tilts are referred to as the <u>centroid</u> position. Traditional systems use a single CCD to sample the entire wavefront resulting in a data bottleneck. In our system, each lenslet will focus only a local portion of the wavefront onto a tilt sensor consisting of a small number of optical detectors, analogue and digital electronics and local centroid processing. The array of tilt sensors will be linked to a matrix processor to reconstruct the estimate of the complete wavefront. Once calculated, the reduced bandwidth wavefront data can then be transferred off-chip. This allows a form of parallel processing to be achieved at each tilt sensor resulting in a data rate independent of the number of tilt sensors employed. A key component in such a final system is the centroid calculation or the angle of tilt. This paper describes the design and characterisation of a real time centroid processor to be used in applications such as wavefront sensing.

2.1 CURRENT CENTROIDING SYSTEMS

Three types of optical front-end devices (sometimes referred to as position sensitive devices) are commonly found in the literature for the detection of a centroid. These are: lateral-effect photodiodes (LEP), sometimes called position sensitive detectors (PSD)[2]; quad cells or quadrant detectors[3]; and finally multi-pixel arrays. Conventional LEPs have high linearity but require a very uniform resistive layer with large sheet resistance, which is not generally available with a standard CMOS process. Linearity may also be affected by contact strips with finite conductivity, and imperfect isolation at the edges of the resistive sheets. Ideally, a LEP should have a double-sided (top and bottom) construction but again this is not possible with a standard CMOS process. Quad cells, as the name suggests, consist of four photodetectors in a 2 x 2 arrangement. A typical device would consist of an array of these quad cells. These devices have simple readout schemes but are not very linear and do not have very good sub-pixel accuracy. With sufficient number of pixels, multi-pixel array systems have very high linearity and good sub-pixel accuracy. Current multi-pixel array systems[4, 5, 6, 7] use an analogue current dividing method to find the centroid which require the use of a linear resistive array. A problem faced by these multi-pixel systems is the mismatch and poor tolerance of the polysilicon resistors in the divider line. The advantage of performing the centroid computation in analogue is in terms of speed and high functional density. However, this traditional advantage is rapidly disappearing as digital CMOS technologies are continuously downscaled resulting in higher and higher speeds and greater functionality per unit area. Digital implementation also benefits from high noise immunity and do not suffer inaccuracies due to the poor tolerance of on-chip analogue components. A generic optical processor, which contains an on-chip photo-detector array and an internal microprocessor, has been designed by Forcheimer[8]. This excellent device, now available commercially by Integrated Vision Products, allows flexible implementation of prototype optical algorithms but due to its generic nature does suffer from the fact that processing time is impaired. It is this multi-pixel approach with on chip CMOS digital processing specifically designed for centroid calculation that is to be exploited for the work presented here.

3. DESIGN PHILOSOPHY

It is well known that the design and fabrication of a mixed analogue and digital ASIC carries the possibility of the design falling outside of the specification and hence more than one fabrication iteration is required. Although excellent analogue simulators exist, photodiodes are not available in the library and integrating these with digital logic requires a mixed analogue and digital simulator. Due to the sensitive nature of analogue circuitry to IC process variations it is inevitable that fine-tuning of the design is required. Consequently, more than one mask iteration is required before a successfully operating circuit can be realised. As a result, the successful design of an optimised optical VLSI processing algorithm at the first mask iteration is fraught with problems and can carry a heavy cost penalty. The design philosophy adopted for our work is therefore to use a two-stage process of a hardware emulation system prior to ASIC fabrication. The hardware emulation system consists of a re-configurable digital device (called a Field Programmable Gate Array or FPGA) and a commercial photodiode array. Once the emulation hardware confirms the satisfactory performance of a design in its intended application, it can then be converted into a mask programmed CMOS integrated circuit. This philosophy, although conservative in its approach, attempts to reduce the number of iterations needed to achieve a successfully operating optical VLSI processor. Due to the re-programmable nature of the FPGA the hardware emulation environment can also be used for many other optical processing algorithms prior to ASIC fabrication.

The work described in this paper explains how the optical front-end array and centroid logic has been implemented in CMOS technology prior to the complete integration of both array and centroid processing onto a single piece of silicon. This work is

one part of a larger project to implement a fully integrated CMOS Shack-Hartmann wavefront sensor. This section describes the centroid calculation, the FPGA hardware emulation system and a CMOS integrated circuit fabricated for implementing the front-end photodetector array.

3.1 CENTROID CALCULATION

The centroid of an array of photo-detectors is expressed in terms of its x and y coordinates, C(x) and C(y). The values of C(x) and C(y) and hence the centroid of the array are found from the "1st moment" equations:

$$C(x) = \frac{\sum r_{xn} I_n}{\sum I_n} ; \qquad C(y) = \frac{\sum r_{yn} I_n}{\sum I_n} ;$$

where r_{xn} is the displacement of each photo-detector from the origin of the array in the x-direction
r_{yn} is the displacement of each photo-detector from the origin of the array in the y-direction
I_n is the light (current) level of each photodetector.

For example consider the 4 x 4 shaded photo-detector array shown in Figure 1 with arbitrary light intensity as shown by the decimal numbers 3, 4, 5, 6 and 7. With these given light levels a centroid position of C(x)=2.53 and C(y)=2.68 would occur.
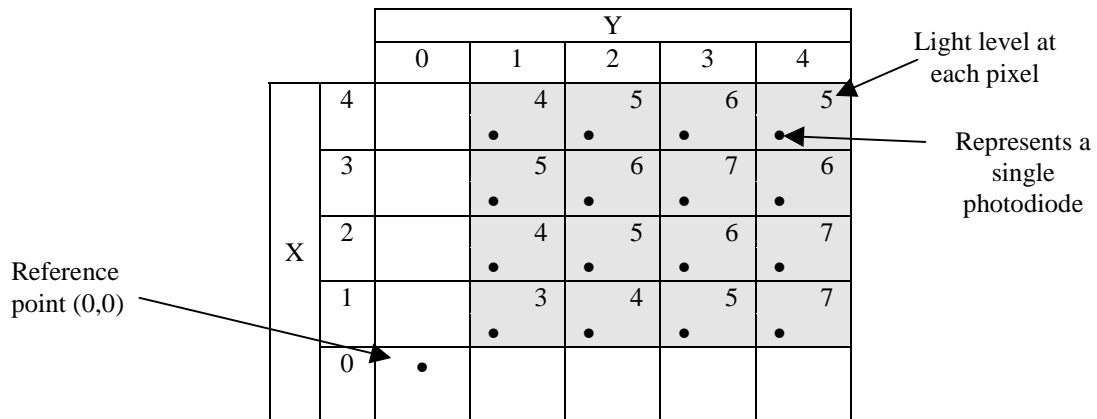

Figure 1. Schematic of photodiode array illustrating light levels for centroid calculation of C(x)=2.53 and C(y)=2.68

If the light levels are represented digitally then these centroid moments can be implemented using the block diagram shown in Figure 2 for the x-coordinate and another duplicate block (not shown) for the y-coordinate. Photocurrent data is clocked in sequentially from each photo-detector and multiplied by a counter (Mod $N^{1/2}$, where N is the number of pixel elements in the array) that holds the position of the detector relative to the reference point in the x direction. The Mod $N^{1/2}$ counter represents this relative position (in the x-direction) from the reference point (r_{xn}). The output of this multiplier is continually accumulated via an adder block and the result is divided by the total photocurrent acquired via a separate and parallel running accumulator. The resultant division represents a 7 bit digital representation of the x centroid coordinate. A second centroid processing block calculates, in parallel, the y-coordinate centroid.
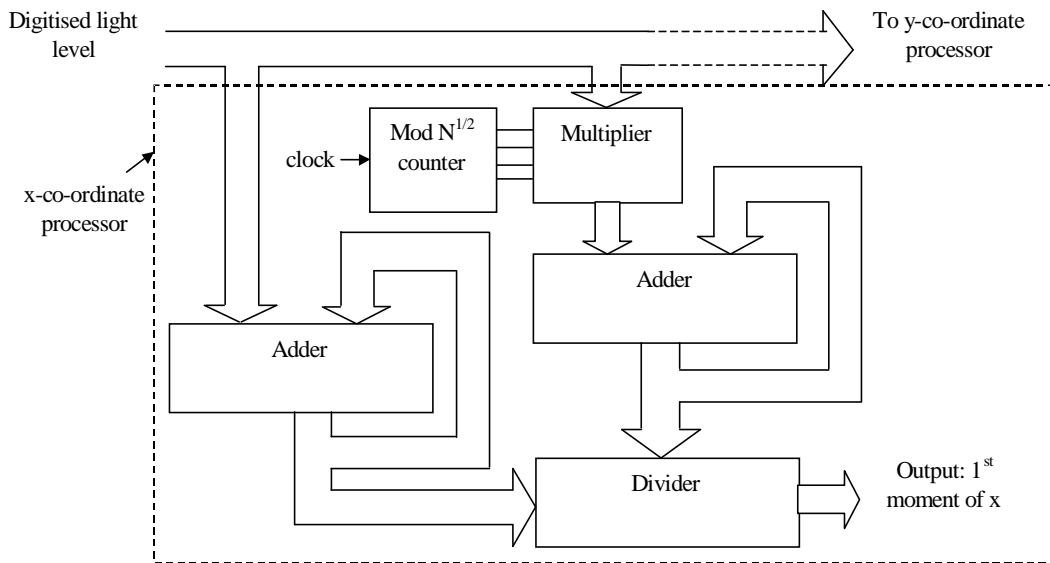
Figure 2. Block diagram of centroid processor in the x-direction

3.2 HARDWARE EMULATION SYSTEM

The hardware emulation system allows optical processing algorithms to be debugged prior to CMOS foundry fabrication. This system, shown in Figure 3, consists of two printed circuit boards: a main motherboard and a smaller daughter board.
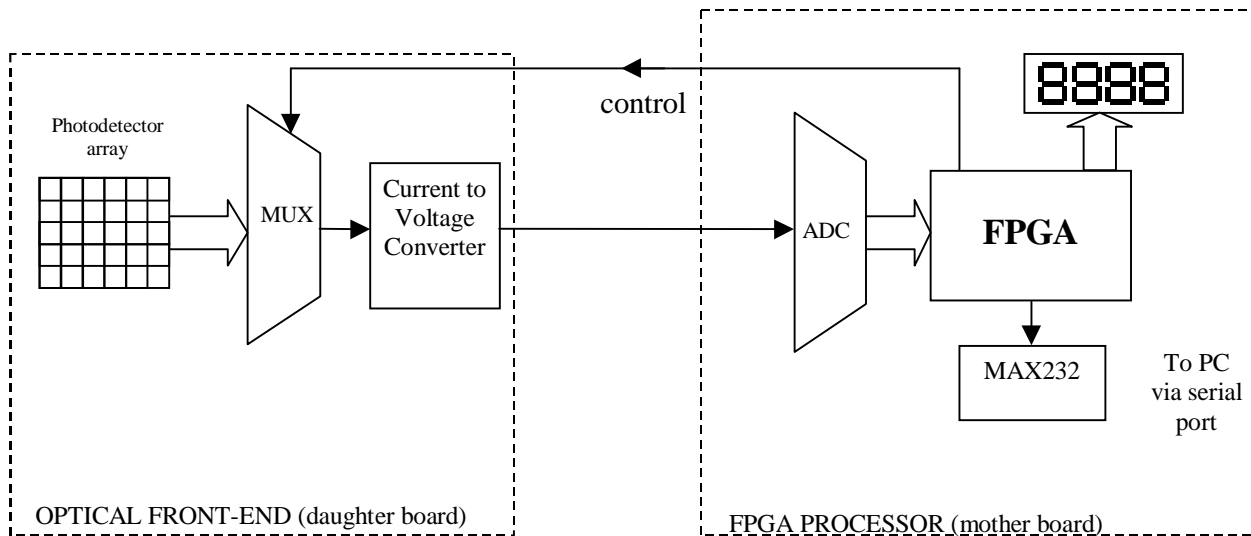

Figure 3: Block diagram of centroid emulation hardware

The motherboard contains a single channel 16 bit analogue to digital converter (ADC), a Field Programmable Gate Array (FPGA), serial PROM for storing the FPGA configuration file, MAX232 for a PC serial interface, LED displays for debug purposes and miscellaneous switches for initiating various test routines under user control. The second, smaller, daughter board contains an optical front end customised for the centroid application and uses a commercially available, 5 x 5, common cathode photodiode array from Centronics (part number MD25-5T).

The FPGA employed on the motherboard is the Xilinx Spartan series device (XCS40-3PQ208C) which contains approximately 40,000 system gates and contains an erasable and hence reusable architecture. This reusable facility allows several iterations of the firmware before transferring to a mask programmable device. This FPGA is programmed via VHDL which, as a high level hardware programming language, maps directly to the digital logic gates on the FPGA. VHDL is a powerful programming language and can handle complex processing and control via a few lines of code. Synthesiser software allows the VHDL design to be easily mapped to both the FPGA and the chosen CMOS IC foundry. Due to VHDL's technology independence, migration to other CMOS foundries, as feature lengths reduce, is easily catered for. The software used to implement the VHDL code on the FPGA is the Xilinx Foundation series 2.1i CAD tools running on a Pentium III 500MHz PC. This software is intuitive to use and allows both pre and post layout simulation so as to check for timing problems.

The centroid is computed by multiplexing each photodiode output into a current to voltage converter on the daughter board. The current to voltage converter simply consists of an op-amp in the transimpedance mode i.e. with a feedback resistance. An op-amp with low input bias current is necessary. The input bias current should be significantly smaller than the photocurrent that is to be converted because the large feedback resistance will convert this input bias current into a dc offset voltage at the output of the op-amp for every pixel. This will significantly affect the centroid algorithm by shifting the centroid position towards the centre. The CMOS amplifier TLC2274 was selected because of its low input bias current of 1pA, its rail-to-rail operation and its low-noise ($9nV/\sqrt{Hz}$). The converted voltage is then digitised by the ADC on the motherboard. Here, the FPGA computes the centroid computation by implementing the block diagram of Figure 2 in VHDL. Each centroid is updated on the FPGA every N+5 clock cycles. Since N, the number of photo-diodes, is 25 and the clock speed is 40KHz then a new centroid is calculated once every 0.75ms (when this design is transferred to a fully integrated mixed analogue and digital process with a 40MHz clock, for example, a centroid will be computed once every 0.75μs). The MAX232 device on the motherboard passes the centroid data via its serial port to a PC at a baudrate of 38KBps thus allowing centroid data to be continuously logged onto disk. Once the emulation hardware confirms the satisfactory performance, the design can be converted into a mask programmed CMOS integrated circuit.

3.3 DESIGN OF ON CHIP CMOS PHOTODETECTORS

This work is the first phase of a three-stage design process to implement a fully integrated CMOS wavefront processor. This first stage involves the design of the CMOS based optical photodetector array. The second phase will integrate both the centroid processing and photodetector array whilst the third and final phase will integrate several centroids onto a single CMOS IC so as to compute the overall wavefront. The aim of this first phase is therefore to replace the commercial Centronics array with our own CMOS photodetector array and again compute the centroid via the previously proven FPGA centroid algorithm.

In a standard CMOS process, several photodetectors exist as a result of the naturally occurring source and drain regions and N and P-type substrates. The cross-sectional difference between each of these is shown in Figures 4a-4d.
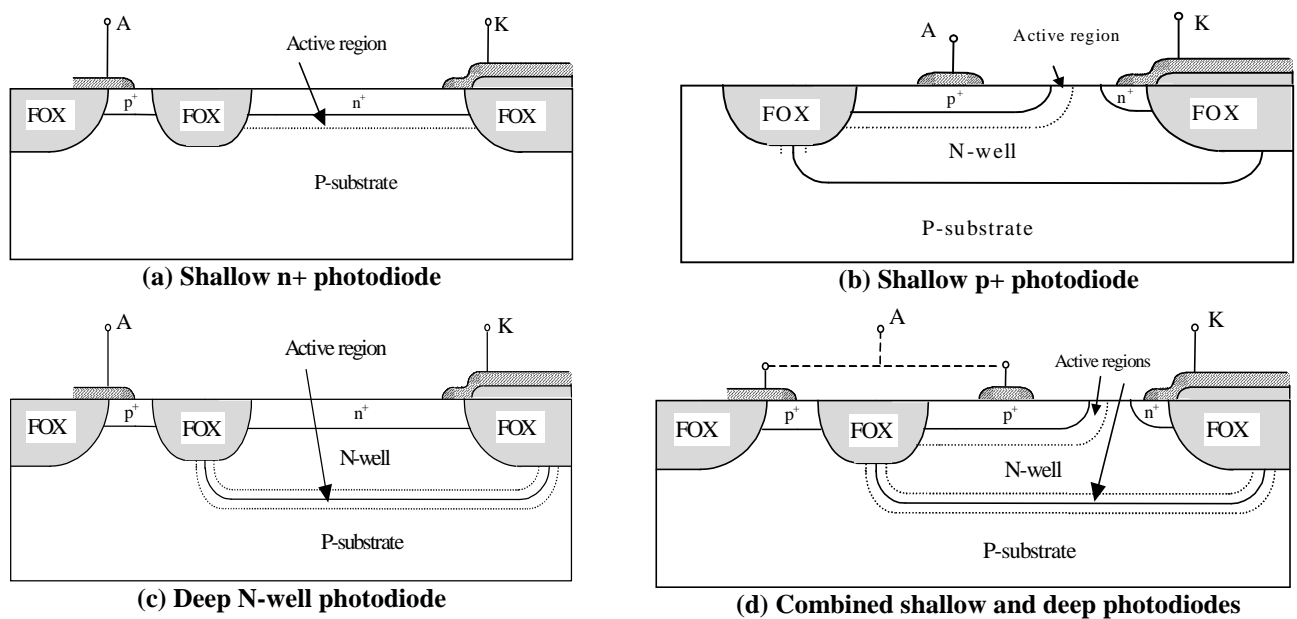

(a) Shallow n+ photodiode

(b) Shallow p+ photodiode

(c) Deep N-well photodiode

(d) Combined shallow and deep photodiodes

Figure 4. Four different photodiode configurations available in a standard CMOS process

Figures 4a and 4b illustrate the shallow (diffusion-substrate or diffusion-well respectively) photodiodes. These have good spectral response at shorter wavelengths, as these wavelengths do not penetrate very far into the substrate. They also possess good substrate noise immunity due to the presence of the deep field oxide (FOX) implants. Figure 4c shows a deep or N-well to p-substrate photodiode. This has good responsivity due to its wide depletion region caused by the relatively low carrier concentration in the n-well and p-substrate. Since it is deep it is also able to collect the minority carriers photogenerated deep in the substrate provided that they are generated within a diffusion length of the depletion region. The deep photodiode has good spectral response at longer wavelengths. This is due to the fact that light of longer wavelength penetrates deeper into the n-well. Figure 4d shows the combination of both deep and shallow photodiodes thus maximising the collection of both short and long wavelength photons. In order to characterise the CMOS process for photosensitivity, all photodiode types were included on the CMOS IC. In addition a 5x5 photo-diode array (pixel size of 100μm square) was laid out on the same chip where each photodetector contained both deep and shallow photodiodes as in Figure 4d. All structures were designed with a guard-ring around every pixel to minimize leakage current to neighbouring pixels.
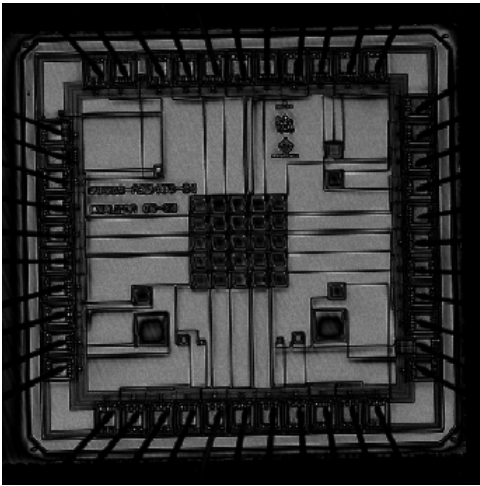

The CAD tools used were Mentor Graphics version C4 running on a Sun Workstation. Schematics were entered via "Design Architect" and layout was implemented using "IC station". CMOS Silicon Libraries (0.7μm mixed analogue and digital) were provided by Mietec Alcatel via Europractice. A photomicrograph of the fabricated device is shown in Figure 5, which clearly illustrates the 5 x 5 photodiode array in the centre of the chip.

Figure 5. Photomicrograph of CMOS photodetector chip

4. RESULTS

4.1 CENTROID MAPS FOR COMMERCIAL PHOTODETECTOR ARRAY

As a test of the VHDL centroid algorithm the centronics photodiode array was connected to the FPGA board and the FPGA was programmed to implement the centroid processing as previously illustrated in Figure 2. A 20μm diameter laser beam (a double YAG laser at 532nm with approximate output power of 0.86mW) was scanned across the array at a speed of 2000μm/sec. Centroid values were computed by the FPGA at about 1.3kHz and serially transmitted in real time to a PC. Figure 6 shows a grey scale map of the centroid values successfully recorded at each position on the array. The dark regions correspond to larger centroid coordinates whilst lighter regions correspond to small centroid coordinates. As expected, as we scan in the x-direction, the x-centroid values increases while the y-centroid values remain constant and vice versa. Since the laser beam size is less than the size of one pixel then a stepped appearance can be seen as the beam moves across the array passing from one discrete detector to another.
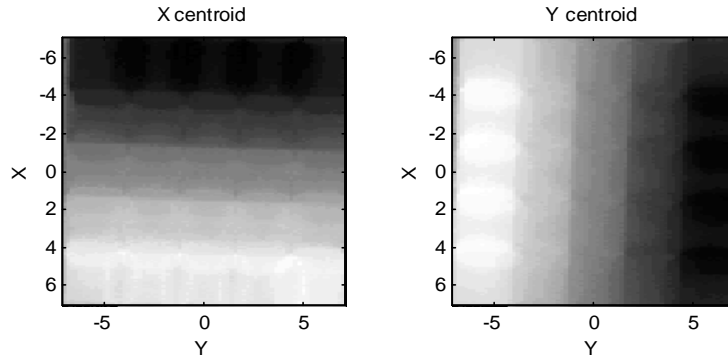
Figure 6. Image map of x and y centroids for the centronics array

4.2 CMOS PHOTODETECTOR ARRAY

The responsitivity of the CMOS photodiodes were recorded under reverse bias using the double YAG laser at 532nm. Responsitivity values of all three diodes varied from 0.36A/W to 0.48A/W. This compares favorably with the Centronics photodiode value of approximately 0.4A/W and previously published material on CMOS photodetectors by Forcheimer[8]. Relative sensitivity was also recorded as a function of wavelength. All three photodiode structures exhibited good sensitivity over the range 450nm to 900nm. The shallow photodiode, as expected, continued to function at short wavelengths since it is able to capture those photons absorbed at shallower depths.

Centroid values were again calculated in real time by the FPGA with the 532nm laser scanned across the custom made CMOS array. Figure 7 shows the y-coordinate centroid values plotted as a function of pixel position for different beam diameter sizes. The array goes from -250um to 250um. Near the edges we can see non-linearity effects as the beam falls off the edge of the array. This effect is more pronounced for larger beam sizes because these will fall off the edge first. For very small beam sizes, we obtain discrete steps in the waveform as we would expect as the beam passes from 1 pixel to another. The steeper rise in centroid value occurs when the beam lands in-between two pixels. As the beam size increases the response becomes more linear in the centre of the array.
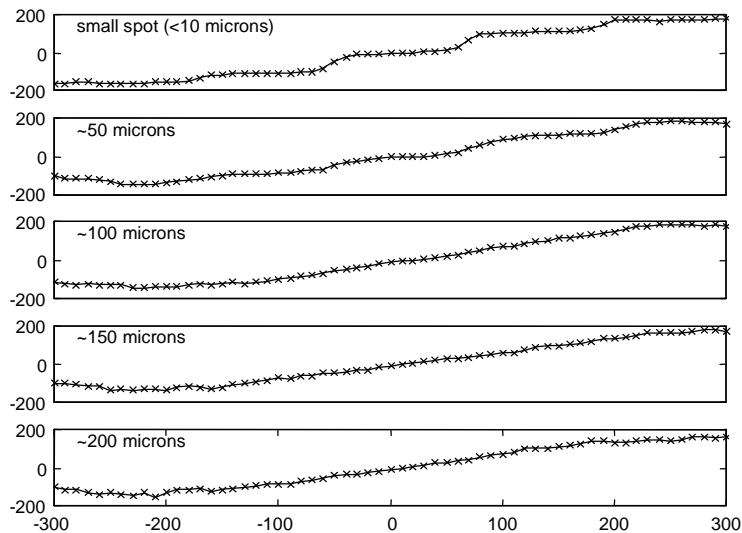

Figure 7. Measured position vs. actual position for different beam sizes

Figure 8 shows the grey scale centroid maps for both the x and y centroid coordinates obtained in real time by the CMOS array via the FPGA. Again the darker regions correspond to large centroid coordinates and vice-versa for light regions. Again we can see the stepped appearance with small beam size and a smoother appearance for larger beam size.
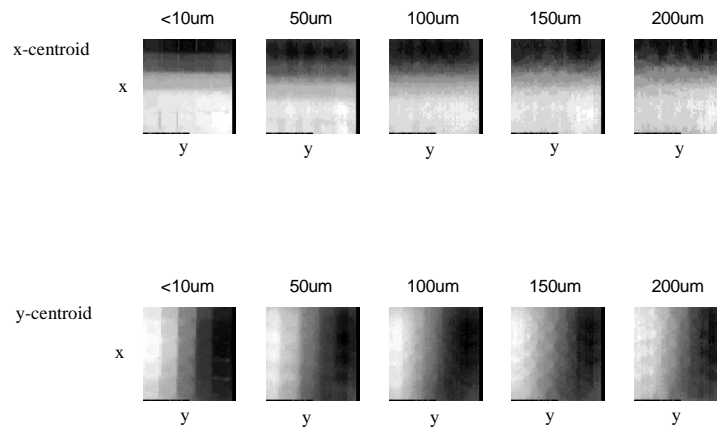

Figure 8. Image map of x and y centroids for different beam sizes

CONCLUSIONS

This paper demonstrates the ability of a custom-made CMOS photodiode array to compute in real-time the centroid of a scanning light beam. Centroid values are computed once every 0.75ms which when transferred to a fully integrated mixed analogue and digital CMOS process operating at a conservative 40MHz will scale to 0.75µs. This rate of update of centroid position is more than adequate for the proposed Shack-Hartmann wavefront sensor. In addition, CMOS photodiodes have been designed and fabricated having sensitivities in the range 0.36-0.48 A/W operating from 450nm to 900nm.

ACKNOWLEDGEMENTS

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