A lock-in pixel for a CMOS Modulated Light Camera

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Abstract

This work describes a CMOS pixel with a logarithmic response suitable for use in a Modulated Light Camera (MLC). The sensor has been designed to detect low modulated light depth (less than 0.5%) at a maximum theoretical frequency of 25 MHz and tested at 1 MHz. The pixel consists of a photodiode, a transimpedance amplifier, a Gilbert cell and an active 150 Hz low-pass filter. It is a compact design suitable for tiling into an array for imaging purposes. This allows the modulated component to be detected at the pixel level thereby allowing a modulated light camera to operate at frequencies far in excess of conventional imagers. We present here the architecture and experimental results from the prototype chip fabricated in a 0.35 µm CMOS process.

1. Introduction

CMOS image sensors allow the realisation of inexpensive parallel processing vision devices using standard VLSI technologies. In this paper we present a lock-in pixel for a CMOS modulated light camera (MLC) capable theoretically of detecting modulated components in the incident light at a frequency of 25 MHz, far in excess of that which is possible with any charge integrating imager. Work previously reported centres around designs operating in the 1-200KHz region [1,2] with the additional work by Bourquin [3] operating up to 1MHz. This latter work employs reduced selectivity at the output via a 35KHz low-pass filter whilst the system reported in this paper uses a 150Hz cut-off.

An MLC can enable single point techniques to become full field thereby offering significant advantages. For instance heterodyne microscopy scanning systems are susceptible to microphonics. The use of an MLC has the potential to acquire an image in a single shot. The MLC pixel presented here can be used to measure both the amplitude and phase components in such a system by simply introducing a 90° phase shift in the reference generator.

The lock-in pixel for a CMOS modulated light camera presented here is faster than standard integrating, charge-to-voltage converting active pixel sensors [4,5]. A typical MLC application for 3D vision time of flight imaging is shown in Fig.1. This uses high frequency modulated light aimed at the source. This light is then detected by the MLC, which extracts the phase and amplitude. The amplitude gives the conventional image and the phase gives the depth of the object. Modulated camera pixels are a basic technology with many applications including:

- optical coherence tomography (OCT) [6]
- ultrasound modulated light tomography [7]
- full field heterodyne interferometry
- 3D vision/range finding (LIDAR – Light Detection and Ranging, Fig. 1)
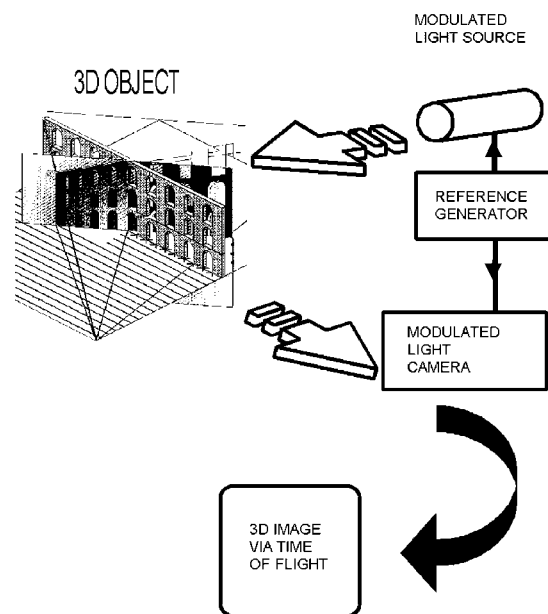

Fig. 1 3D time of flight imaging using a modulated light camera.

2. Chip description.

The MLC integrated circuit has been designed and fabricated in the AMS 0.35 µm (CSI) CMOS process. We have a complete pixel, which is described below plus test photodiodes on the same chip thereby allowing the performance of the photodiode itself to be characterised.

A block diagram of the presented MLC pixel sensor is shown in Fig. 2. The chip integrates a logarithmic sensor (50 µm x 50 µm photodiode and diode-connected transistor) with a transimpedance amplifier (TIA)

followed by a buffer (buffers are not shown in Fig. 2). The output of the sensor is then converted to a differential signal and amplified before being fed to the differential input of a mixer where it is multiplied with a reference local oscillator (LO). This forms a phase sensitive signal path. A low pass filter at the output of the mixer provides lock-in detection that removes unwanted components from the signal spectrum.
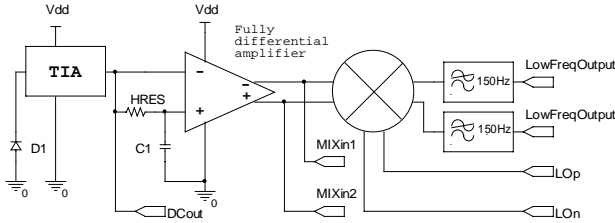

Fig. 2 Block diagram of the modulated light camera pixel.

The transimpedance amplifier (TIA) is a crucial element because the speed, sensitivity, and signal-to-noise ratio (SNR) characteristics of the whole lock-in pixel are mainly determined by its performance. However, the design of the TIA (shown in Fig. 3) requires a number of tradeoffs between high gain, wide bandwidth, low noise and low power consumption. The bandwidth and sensitivity characteristics of the TIA are primarily determined by the total input capacitance whose main component is the junction capacitance of the photodiode. Here we use an n-well-substrate ("deep") photodiode, which has a relatively low capacitance compared with other p-n junctions available in a standard CMOS process. The deep photodiode has the advantage of being able to collect electrons generated deep within the substrate thus improving light to current conversion and sensitivity. However, a disadvantage is that it can be sensitive to substrate noise and crosstalk from neighbouring pixels.

Due to the local feedback the input stage (see Fig. 3) functions like a current-buffer that has higher efficiency than a diode-connected transistor. Consequently, the feedback TIA buffers the photodiode capacitance thereby increasing the bandwidth. This bandwidth increases with increasing DC light power although this reduces the small signal transconductance gain of the input stage.
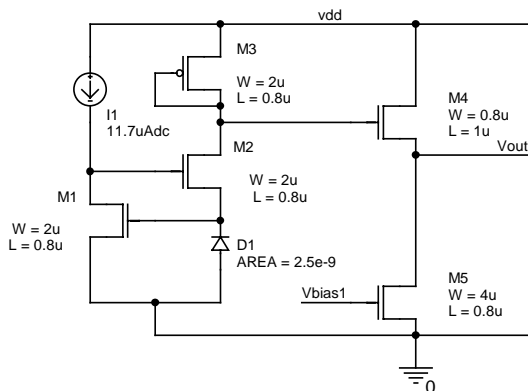

Fig. 3 Front-end transimpedance amplifier (TIA) and source follower.

The single-ended output of the TIA input stage is converted to a differential signal using an R-C filter and a fully differential amplifier (see Fig. 2). As a capacitor we use the gate capacitance of a MOS transistor operating in strong inversion. The resistor is implemented using a "horizontal resistor" (HRES) circuit described in [8]. The circuit allows the realisation of a large value resistance in a small silicon area - significantly smaller than standard resistors available in AMS CSI process. The DC background light is rejected by the high common mode rejection ratio of the differential amplifier. The amplifier is a fully differential design that rejects the common-mode noise of the substrate coupling and inter-channel coupling.

There are many different mixer circuit topologies and implementations that are suitable for use in this application. That used here is based on a double balanced four-quadrant Gilbert cell topology. This structure has the most desirable characteristics in terms of isolation and harmonic suppression due to its balanced structure. It rejects common mode digital clock noise, which is important for our design, as it will be integrated with digital components. The output is the mixed product of two inputs, namely the high frequency input (RF) and the local oscillator (LO). This output therefore contains the sum and difference of the two input frequencies. Since both input frequencies are the same the output contains two components: a DC voltage and a component whose frequency is twice the input frequency. The DC component is filtered from the output of the mixer by a low-pass filter and allows the amplitude and phase of the modulated signal to be calculated. Noise present at the signal frequency in the mixer input goes through a similar process as the signal itself but it is also added to the noise generated in the active devices and resistive components in the mixer. Mixers can contribute significantly to noise due to the signal loss in the switching and due to the noise transferred from multiple frequency bands to the output. The harmonics of the LO signal mix the noise directly to the baseband. Ideally the loss in the switching elements of double-balanced switching mixer is 3.9 dB, but this value is very often much higher. This is an indirect effect of the gain degradation due to the non-ideal LO polarity switching [9]. There are usually three noise contributors in a mixer: the input stage, the time varying switching stage and the output stage. Because in our application the signal is mixed down to DC and then filtered with a very narrow band low-pass filter, it can be expected that the main noise contributors apart from the front-end are the mixer and low-pass filter.

The output of the mixer is differential. This will not be necessary in a final design when tiling the pixel into an array. At this stage we have kept the output differential as this provides a larger measurable voltage swing at the external output pads. Integrating the differential to single ended converter will of course save half of the space occupied by the filters thus making the array design more compact and significantly improving the fill factor.

The low-pass filter is designed as an OTA-C circuit as shown Fig. 4. Here the 3 dB cut-off frequency is calculated from:

$$f_{3dB} = \frac{Gm}{2\pi C} \qquad (1)$$

where G_m is a transconductance of the entire OTA and C is the capacitive load. For a 3 dB cut-off of 150 Hz and a transconductance of 65nA/V a capacitance of the order of 70pF is required.
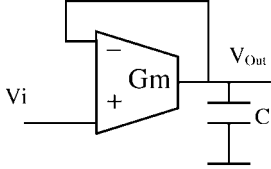
Fig. 4 First order low-pass OTA-C filter.

A low–pass filter with a cut-off frequency as low as possible is desired when designing a lock-in amplifier. A cut-off frequency (3 dB) of 150 Hz was chosen as this allows us to build a filter without applying more complex design techniques and additional circuits such as impedance scalers. The 150 Hz cut-off frequency removes a significant amount of noise and provides good lock-in detection. A G_m of a value of 65nA/V is difficult to achieve using standard differential transistor pair. Moreover, such a circuit suffers from distortion, reduced dynamic range and high noise, which are all key parameters in this type of application. In our pixel we use a current division OTA shown in Fig. 5 with source degradation to improve the linearity [10].
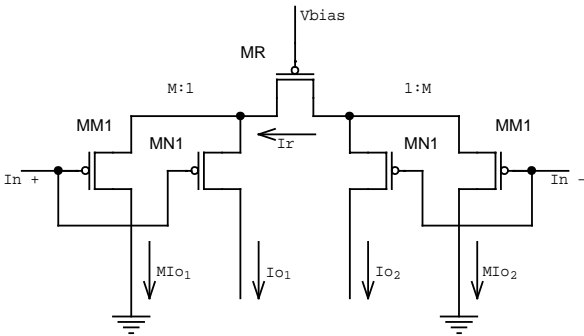
Fig. 5 Current division OTA [10] used to form a low-pass filter shown in Fig. 4.

Transistor MM1 is M times the size of MN1 and hence $g_{MM1} \gg g_{MN1}$ and only a small part of the current (M times less than in the conventional OTA) is collected at the output of a differential pair. Increasing the factor M will reduce the transconductance, G_m, thereby realising an OTA-C filter with a very low cut-off frequency using a reasonable size capacitor of 70 pF. Simulation results indicated a 3 dB cut-off frequency of 156 Hz. P-channel MOSFETs were used rather than n-channel for this low pass filter since these have a lower 1/f noise. Note that when using this current division technique noise is reduced by the same factor as G_m. The most important sources of noise are the transistors MN1 and the load transistors that collect the current from transistors MN1. To further minimise the noise these transistors are

designed as devices with a large gate area, which also reduces the 1/f noise.

Careful layout design of all stages is required since the pixel contains sensitive circuits such as a front-end, single-ended to differential converter as well as noisy mixer circuits. Separate bias circuits for sensitive input stages and noisy nonlinear blocks are used. The chip will be normally exposed to laser and ambient light. Thus it is necessary to protect the active transistors from light. This is achieved by adding a light blocking layer using the third metal. First and second metal layers are used mainly to connect the circuits; however wherever possible they are also used as shielding layers and are part of a distributed capacitance that helps to filter the supply voltage. The final layout is shown in Fig. 6.
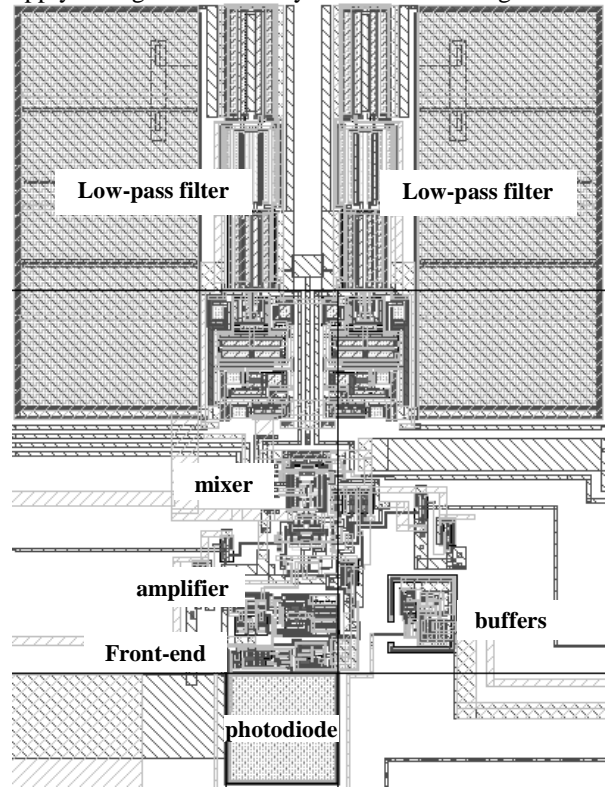
Fig. 6 Layout of the presented MLC pixel.

3. Experimental results.

Experiments were carried out to verify the characteristics of the individual camera building blocks and the entire pixel. To perform the tests we used a semiconductor laser diode with a wavelength of 532 nm. The measurement was carried out by attenuating a laser beam with neutral density filters and with the beam focused on the photodiode to a spot size of approximately 5 microns. The responsivity in the centre of the photodiode was measured as 0.32 A/W. Tests were performed on the full MLC pixel using a modulating semiconductor laser diode of a wavelength of 670 nm. This 330nW light source was modulated at 1 MHz with an initial modulation depth of 10%. Although the pixel can operate at much higher frequency, 1 MHz was chosen in order to use readily available test equipment. The modulated laser beam was again focused on the

photodiode to a spot of about 5 μm. The frequency of the local oscillator reference was then swept from 10 Hz to 4.5 MHz. The measured normalised spectral response from the MLC output is shown in Fig. 7. The signals with frequency different than the lock-in frequency are rejected. With this light intensity the mixer works close to saturation and therefore due to non-linearities the circuit shows some response to harmonics of the fundamental carrier. Reduction of the modulation depth demonstrated the disappearance of these harmonics and it was found that the system would operate satisfactorily down to modulation depths of 0.5% – a limit set by the measurement accuracy of the equipment and not the pixel itself. Figure 8 shows a close-up of the 1 MHz fundamental component, illustrating the very narrow response of the lock-in. The width of this component corresponds to the low-pass filter cut-off frequency. As can be seen this method of detecting modulated light offers a high selectivity and makes it possible to recover low signals buried within noise.
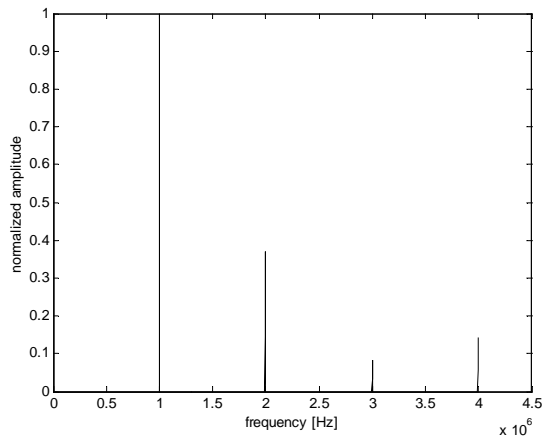

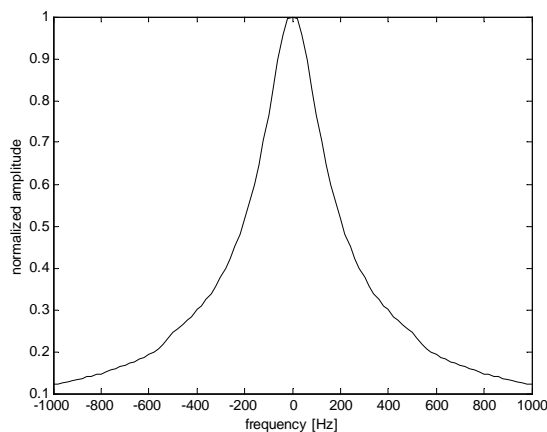**Fig. 7 The low-pass filter output voltage as a function of the local oscillator frequency.**

Fig. 8 Close-up of the fundamental 1MHz component from Fig. 7 – centred at 1MHz.

4. Conclusions.

A lock-in pixel for a CMOS modulated light camera has been presented. This device is capable of detecting modulated light with a modulation depth of 0.5% at the frequency of 1 MHz as used in our experiments and has been simulated to work at maximum frequency of 25 MHz. The presented pixel is scalable to an array of pixels. The layout shown in Fig. 6 has a size of 275 μm x 360 μm. It is worth noting that this pixel is not yet optimal and can be made considerably more compact (at the time of writing this paper we have submitted for fabrication a 2 x 2 lock-in pixel array with quadrature mixer and two low-pass filters integrated at a pixel level for proof of scaling principle. Here, a single pixel has a size of 86 μm x 86 μm with a photodiode of a size 30 μm x 30 μm). Buffers and some bias circuits will not be necessary when making an array and are present only in this test pixel to provide observability of each stage. The cut-off frequency of the low-pass filter will have to be increased to match the array size and required frame rate, which will significantly trim down the pixel size because of the smaller capacitance, needed to realise the filter with higher cut-off frequency compromising lock-in performance. The fill factor can be improved by using a microlens array. The 0.35μm CMOS process is a low voltage, 3.3V process, and as a result the complete pixel draws only 180 μA of current (excluding output buffers).

Acknowledgment

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