A lock-in pixel for a CMOS Modulated Light Camera

Przemyslaw R. Dmochowski, Barrie R. Hayes-Gill, Matthew Clark, John A. Crowe, Mike G. Somekh, and Steve P. Morgan

***Abstract*—This paper describes a pixel with logarithmic response suitable for use in a Modulated Light Camera. The sensor has been designed to detect low modulated light depth (less than 0.5%) at frequencies around 2 MHz. The pixel consists of a photodiode, a transimpedance amplifier, a Gilbert cell and an active 150 Hz low-pass filter. It is a compact design suitable for tiling into an array for imaging purposes. This allows the modulated component to be detected at the pixel level thereby allowing a modulated light camera to operate at frequencies far in excess of any conventional imager.**

We present here the architecture and experimental results from this prototype chip fabricated in a 0.35 μm CMOS process.

***Index Terms*—Active Pixel Sensor, APS, CMOS Image Sensor, Modulated Light Camera.**

I. Introduction

CMOS image sensors allow the realisation of inexpensive parallel processing vision devices using standard VLSI technologies. CMOS imaging technology enables a whole new class of imaging products because of its ability to integrate additional electronics on-chip with low power and low cost. In many imaging applications CMOS sensors are now widely used and have replaced CCD technologies. In addition to their use in traditional applications CMOS allows the integration of local processing at each pixel thereby removing restrictive limitations found in conventional imagers. In this paper we present a lock-in pixel for a CMOS modulated light camera (MLC) capable of detecting modulated components in the incident light at 2MHz, far in excess of that which is possible with any charge integrating imager. Work previously reported centres around designs operating in the 1-200KHz region [1]-[4] with the additional work by Bourquin [5], [6] operating up to 1MHz. This latter work employs reduced selectivity at the output via a 35KHz low-pass filter whilst the system reported in this paper uses a 150Hz cut-off.

Modulated camera pixels are a basic technology with many applications for instance:

- optical coherence tomography (OCT) [7]
- ultrasound modulated light tomography [8]
- full field heterodyne microscopy
- 3D vision/range finding [LIDAR]

An MLC can enable single point techniques to become full field thereby offering significant advantages. For instance heterodyne microscopy scanning systems are susceptible to microphonics. The use of an MLC has the potential to acquire an image in a single shot.

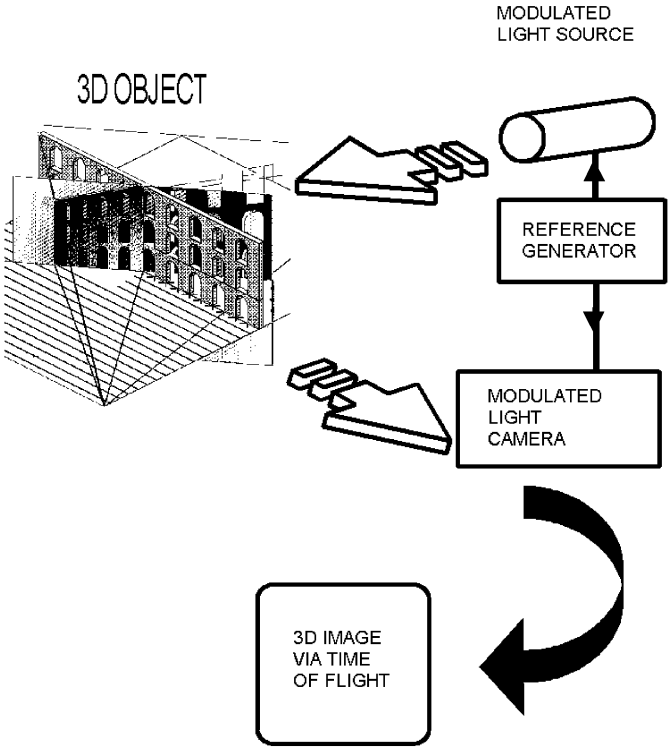

Fig. 1 3D time of flight imaging using a modulated light camera.

The lock-in pixel for a CMOS modulated light camera presented here is faster than standard integrating, charge-to-voltage converting active pixel sensors [9,10]. A typical MLC application for 3 D vision time of flight imaging is shown in Fig. 1. This uses high frequency modulated light aimed at the source. This light is then detected by the MLC, which extracts the phase and amplitude. The amplitude gives the conventional image and the phase gives the depth or range of the object. The MLC presented here can be used to measure both the amplitude and phase components in such a system by simply

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introducing a 90^o phase shift in the reference generator.

II. CHIP DESCRIPTION

The MLC integrated circuit has been designed and fabricated in the AMS 0.35 µm (CSI) CMOS process. We have a complete pixel, which is described below plus test photodiodes on the same chip thereby allowing the performance of the photodiode itself to be characterised.

A block diagram of the presented MLC pixel sensor is shown in Fig. 2. The chip integrates logarithmic sensor (photodiode and diode-connected transistor) followed by a buffer – not shown in Fig. 2. The output of the sensor is then converted to a differential signal and amplified before being fed to the differential input of a mixer where it is multiplied with a reference local oscillator (LO). This forms a phase sensitive signal path. A low pass filter at the output of the mixer provides lock-in detection that removes unwanted components from the signal spectrum.

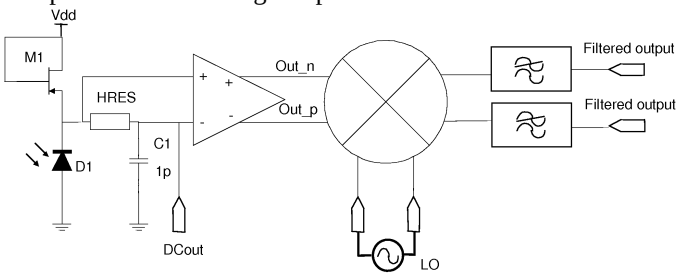

Fig. 2 Simplified block diagram of presented sensor.

A. Pixel sensor

The pixel current to voltage structure is shown in more detail in Fig. 3. A 50µm x 50µm n-well/p-substrate photodiode (D1) was used with a diode connected MOSFET (M1). The transistor M1 conducts the photocurrent and with a low light power (< 30nW) operates in the subthreshold or if the light power is large enough (> 10µW) it can operate in saturation [11]. The pixel output voltage, which varies with illumination intensity, is then buffered via a source follower (M2, M3).

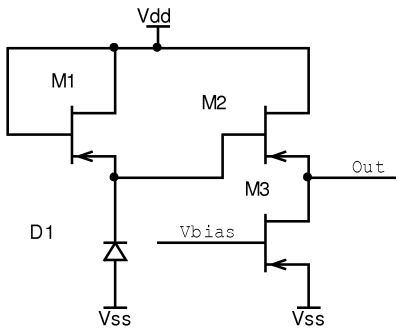

Fig. 3 Logarithmic active pixel sensor structure.

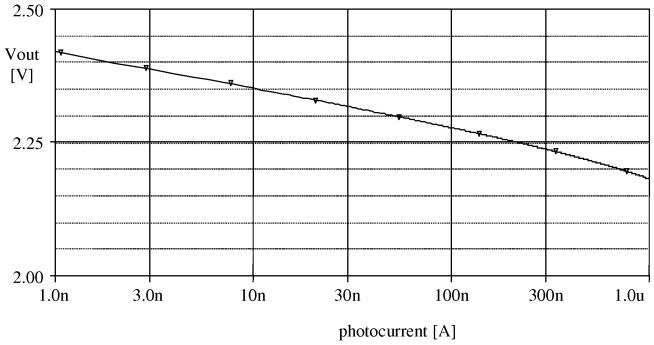

Fig. 4 The simulated logarithmic photosensor characteristic. The output voltage *Vout* (at the output of HRES) decreases approximately logarithmically with increasing light intensity. The slope is approximately 75mV/decade.

Unlike the integrating reset pixel [9] the pixel output in the logarithmic amplifier (Fig. 3) is continuously available. In addition the diode connected transistor having a logarithmic response offers a wide optical dynamic range - see Fig. 4. The typical focused mean power of the laser to be used was 330nW. Given that the typical response of the CMOS photodiode is approximately 0.3 A/W [9] then the DC operating point will be at 100nA of photocurrent. From Fig 4 a small signal voltage swing of 250µV/nW of light intensity is expected. Hence with a modulating current of 10nA an AC small signal swing of 7.5mV is obtained.

B. Amplifier and single-ended to differential converter

The output from the pixel sensor is single-ended whilst the mixer requires a differential input voltage hence a single-ended to differential converter is required. The overall converter and amplifier are integrated and their architecture is shown in Fig. 5. The converter consists of two single ended output operational transconductance amplifiers (OTA) combined into one differential output stage (Fig. 6). The differential amplifier also provides wide bandwidth, low noise and ease of biasing. This structure is used in open loop configuration.

Typically, in designing a good transconductance amplifier, the main tradeoffs that need to be considered are sensitivity due to noise, speed (bandwidth) and transconductance gain. The gain-bandwidth product is usually a figure of merit to consider when evaluating the performance of a transconductance amplifier. The gain of a single stage [11] can be calculated as:

$$Av = -g_{m7}(r_{07} \parallel r_{05}) \tag{1}$$

where, g_m and r_{05}, r_{07} are small signal transistor transconductance and output resistance respectively. These terms are given by the equations:

$$r_{05}, r_{07} = \frac{|V_A|}{I_D} \tag{2}$$

$$g_{m7} = \frac{2I_D}{|V_{GS}| - |V_t|} \quad (3)$$

where V_A is the early voltage, I_D is the transistor's M7 DC drain current, V_{GS} is the DC gate-source voltage and V_t is the threshold voltage.

The voltage gain with transistor's M5 (Fig. 6) DC drain current set at 3μA is approximately 33dB from (1) using the AMS process parameters. Simulation results indicate a confirmation of this gain and satisfactory operation at 2MHz resulting in a gain bandwidth product of better than 90MHz.

The converter is formed by connecting the inverting input of the first transconductance amplifier to the non-inverting input of the second amplifier. The second pair of inputs is connected to the output of a simple RC low-pass filter. This filter is required to bias the second input pair of the differential amplifier. The RC filter was set to have a 10 dB attenuation at 1.5 MHz. This frequency has been chosen as the typical operating frequency for the presented chip.

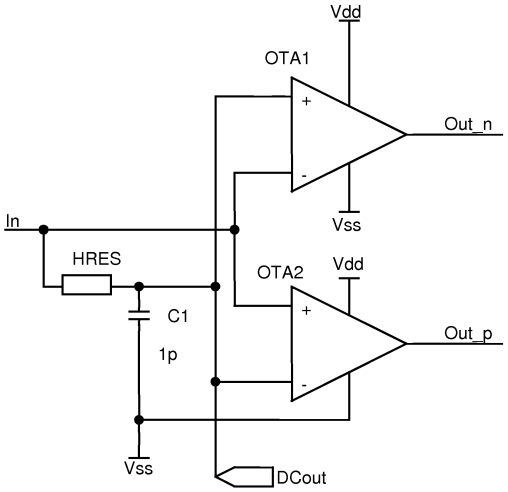

Fig. 5 Amplifier and single-ended to differential converter.

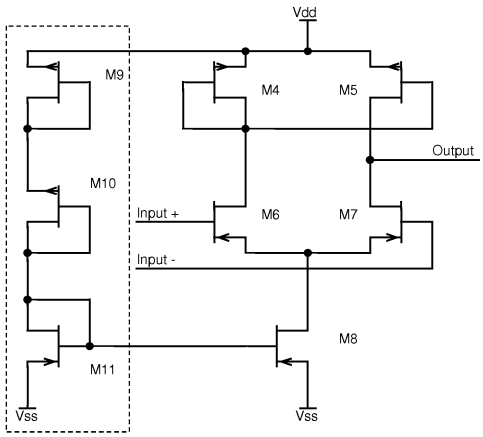

Fig. 6 One stage of the operational transconductance amplifier (OTA) with differential inputs and single ended output. The single-ended to differential amplifier (see Fig. 5) consists of two identical amplifiers. The bias circuit (shown dotted) is common for both amplifiers.

The RC filter has been designed using a capacitor (gate capacitance) and a device called a horizontal resistor (HRES) [12]. The circuit for HRES is shown in Fig. 7a and consists of two MOS transistors in series with separate bias voltages. The on-resistance of these two transistors is dictated by the bias voltages V1 and V2. Setting small values of V1 and V2 produces large values of on-resistance in a relatively small area. The DC current flow in this circuit is given by reference [12] as:

$$I = I_0 * e^{\frac{V_{1,2}}{n*V_T}} * \tanh\left(\frac{V_{in} - V_{out}}{2}\right) \quad (4)$$

where V_T=kT/q, I_0 and n are process dependent parameters. However, in this particular case the load is the gate of an MOS transistor and hence the DC current flow is zero. As a result the DC voltage drop down the chain is also zero and therefore we can use a single common bias voltage instead of two separate bias supplies, V1 and V2. The resulting circuit is shown in Fig 7b. The common gate bias voltage in this case is the buffered common reference point of transistors M12 and M13.

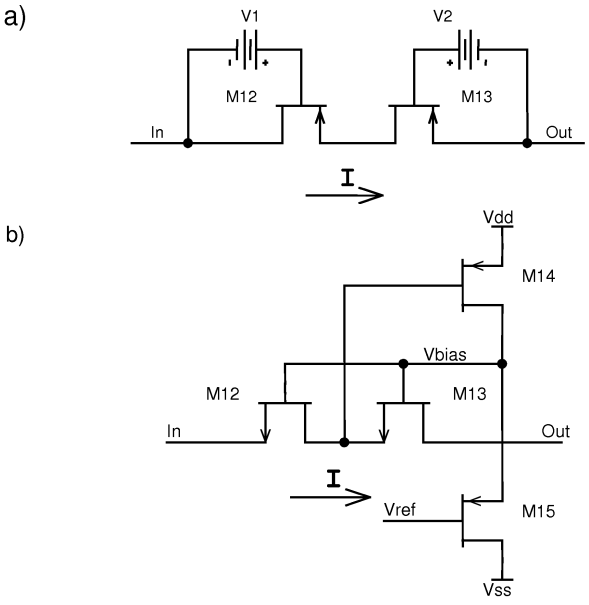

Fig. 7 Horizontal resistor circuit a), practical implementation b).

The horizontal resistor structure used consists of only four minimum size transistors and simulation results indicate a small signal resistance of the order of 0.5MΩ with the bias arrangement shown in Fig 7b. To achieve a 10dB attenuation at 1.5MHz would require a capacitance of approximately 1pF. For this we use the gate capacitance of an NMOS device. This allows us to minimise the silicon area used because of its higher capacitance (4.46fF/μm^2) than the standard poly to poly capacitance (0.86fF/μm^2).

C. Mixer

There are many different mixer circuit topologies and implementations that are suitable for use in this application [13]. The circuit approach used here is based on a double balanced four quadrant Gilbert cell topology. The Gilbert cell structure has the most desirable characteristics in terms of isolation and harmonic suppression due to its balanced structure. It rejects common mode digital clock noise, which is important for our design as it will be integrated with digital components. The output is the mixed product of two inputs, namely the high frequency input (RF) and the local oscillator (LO). This output therefore contains the sum and difference of the two input frequencies. Since both input frequencies are exactly the same the output contains two components: a DC voltage and a component whose frequency is twice the input frequency. The DC component is filtered from the output of the mixer by a low-pass filter and allows the amplitude and phase of the modulated signal to be calculated. The transistor schematic of the Gilbert cell mixer is shown in Fig. 8. Source degeneration in the tail of the differential amplifier section was not applied. Thus, the mixer configuration offers better conversion gain and noise figure rather than linearity.

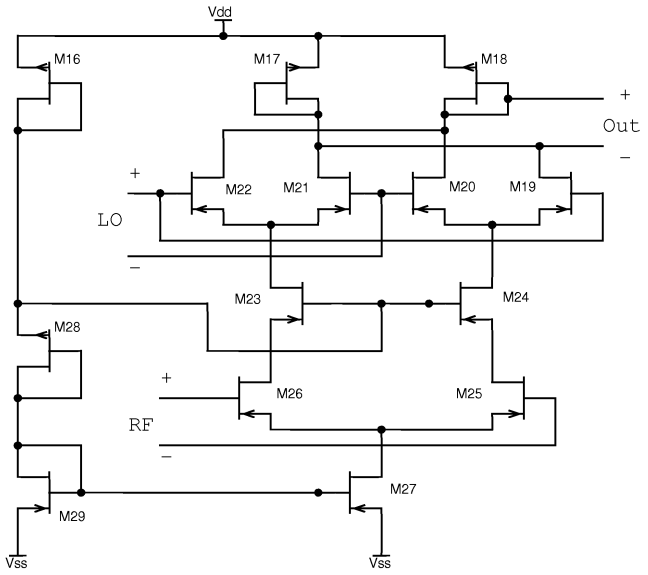

Fig. 8 Schematic of a Gilbert cell mixer.

A Gilbert cell is a differential amplifier, which drives a balanced switching cell. The differential input stage provides gain and determines the noise figure and signal handling performance of the mixer. Assuming ideal transistor switching, the differential mixer transconductance, $g_{m\text{-}mix}$, can be related to the LO MOSFETs' small signal transconductance as [14]:

$$g_{m-mix} = \frac{g_{m21}}{\pi} \tag{5}$$

where g_{m21} is the small signal transconductance of one of the LO MOSFETs. The conversion gain for the Gilbert cell mixer (G_c) can be written in terms of $g_{m\text{-}mix}$, as [14]:

$$G_C = \frac{g_{m-mix} R_L}{1 + g_{d-mix} R_L} \tag{6}$$

where $g_{d\text{-}mix}$ is the mixer drain conductance and R_L is the load resistance. In the presented mixer cell the load resistance forms two diode connected MOS transistors (M17 and M18). These have an equivalent load of g_{m17}^{-1} and g_{m18}^{-1}, which are relatively small. Hence in order to obtain a reasonable conversion gain (G_C) requires the small signal transconductance (g_m) of the LO MOSFETs to be large. This is achieved by using a large width to length ratio of the order of 10 for these transistors.

C. Low-pass output filter

The differential output signal from the mixer is finally filtered by a first order low-pass filter so as to obtain the required DC signal. Low-pass filters with very low cut-off frequency usually require large values of capacitors and large resistors – highly unsuitable for integrated circuits. An alternative that avoids large resistors is to use an OTA-C circuit [15].

To form an OTA-C filter the inverting input of the OTA is connected to its output and a capacitor load as shown in Fig. 9. The 3dB cut-off frequency of the circuit shown in Fig. 9 can be calculated from:

$$f_{3dB} = \frac{Gm}{2\pi C} \tag{7}$$

where *Gm* is the overall transconductance for this amplifier.

A low–pass filter with 3dB cut-off frequency as low as possible is desired. A cut-off frequency of 150Hz was chosen as this allows us to build a filter without applying more complex design techniques and additional circuits such as impedance scalers. The 150Hz cut-off frequency removes a significant amount of noise and provides good lock-in detection. A transistor with W=84μm and L=185μm has a gate capacitance in order of 70pF. From (7) we can see that in order to implement a low-pass filter with a 150Hz cut-off frequency a transconductance Gm of approximately 65 nA/V is required. Such a small value of Gm is difficult to achieve using the structure shown in Fig. 6. Moreover, this circuit suffers from distortion, reduced dynamic range and high noise, which are all key parameters in this type of application.

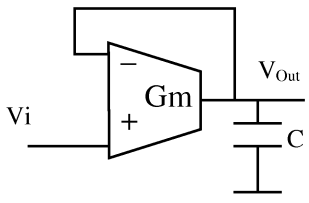

Fig. 9 First order low-pass OTA-C filter.

An alternative OTA circuit, shown in Fig. 10, was used to obtain the small transconductance required. This circuit uses a current division technique [16]. Transistor MM1 is M times the size of MN1 and hence $g_{MM1} >> g_{MN1}$ and only a small part of the current (M times less than in the conventional OTA

shown in Fig. 6) is collected at the output of a differential pair. Increasing the factor M will reduce the transconductance, Gm, thereby realising an OTA-C filter with a very low cut-off frequency using a manageable capacitor. To maintain good linearity we use source degeneration via MR [9].

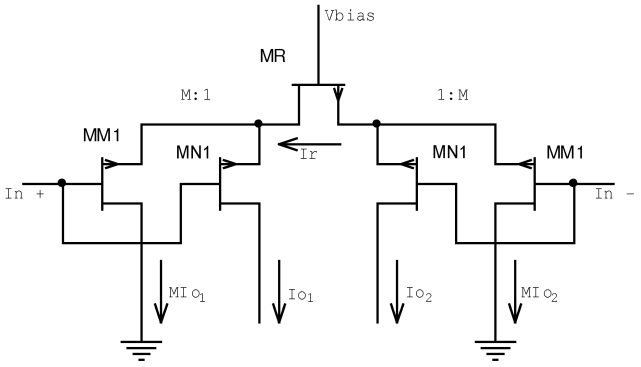

Fig. 10 Current division OTA for low frequency applications [16] used to form a low-pass filter shown in Fig. 9.

P-channel MOSFETs were used rather than n-channel for this low pass filter since these have a lower 1/f noise [16]. Note that when using this current division technique noise is reduced by the same factor as Gm. The most important sources of noise are the transistors MN1 and the load transistors that collect the current from transistors MN1. To further minimise the noise these transistors are designed as devices with a large gate area which also reduces the 1/f noise.

D. Layout

The chip contains very sensitive input circuits such as a front-end, single-ended to differential converter as well as noisy circuits such as a mixer. Therefore careful layout design is crucial. Separate bias circuits for sensitive input stages and noisy nonlinear blocks are used. A shielding ring is designed around every differential pair to protect transistors from noise propagated through the substrate. Dummy transistors help to preserve good matching. During tests the chip will be exposed to laser light. Thus it is necessary to protect the active transistors from light. This is achieved by adding a protective layer using the third metal layer. First and second metal layers are used mainly to connect the circuits, however wherever possible they are also used as shielding layers and are part of a distributed capacitance that helps to filter the supply voltage. The entire layout is shown in Fig. 11.

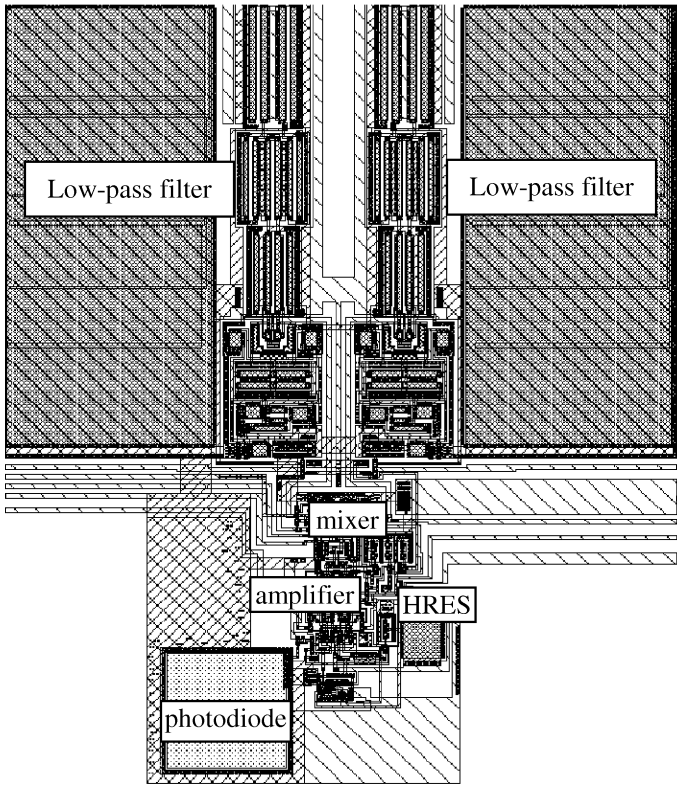

Fig. 11 Layout of the entire pixel, that includes photodiode, amplifier, mixer and 150 Hz low-pass filter.

III. EXPERIMENTAL RESULTS

Experiments were carried out to verify the characteristics of the photodiode, the individual camera building blocks and the entire pixel.

Firstly, the response of a 100μm x 100μm standalone n-well/p-substrate photodiode was measured and the test results are shown in Fig. 12. The upper plot shows a greyscale map of the sensitivity of the photodiode (centred at x=230μm, y=200μm) in response to a focussed 532nm laser scanned across the device in both the x and y directions. The lighter grey responses outside of the device are caused by crosstalk induced by neighbouring photodiodes that were left floating. This crosstalk is easily removed by ensuring that these devices are not left floating and are either grounded or reverse biased. The lower plot shows a single scan in the x-axis across the photodiode at y=200μm. The responsitivity in the centre of the photodiode was calculated as 0.32 A/W. This is slightly below the theoretical value of 0.4 A/W possibly due to the passivation layers used in this CMOS process.

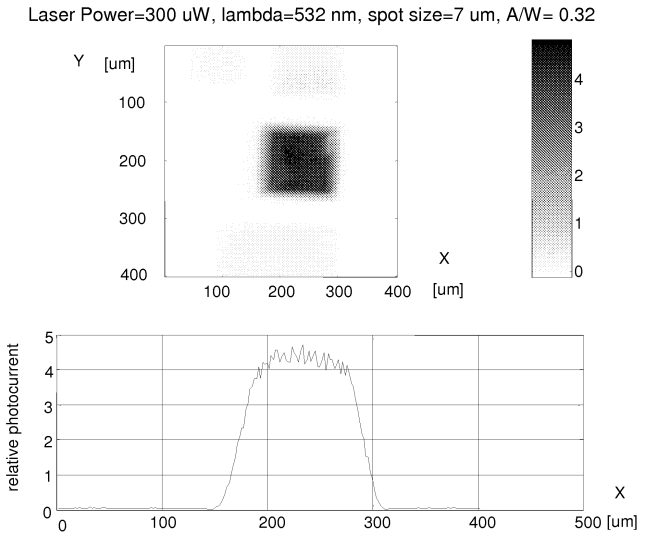

Fig. 12 The measured photocurrent response of the photodiode. Test photodiode size is 100 x 100 µm. The bottom graph shows a line scan along the x-axis in the centre of the photodiode.

The response of the pixel sensor front-end to DC unmodulated light is shown in Fig. 13. The figure shows buffered measured output voltage at "*Dcout"* (Fig. 2) for eight individual chips. These have similar responses and compare well with typical simulated results - the simulation over worst case process corners is also shown.

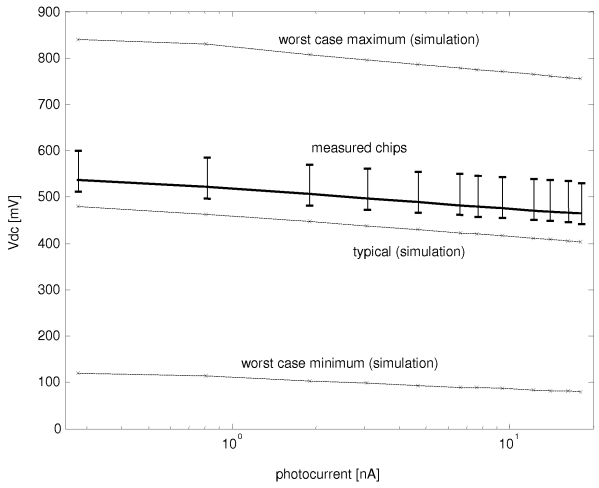

Fig. 13 The logarithmic response of the pixel sensor front-end to DC unmodulated light.

Tests were performed on the full MLC using a 330nW light source modulated at 1 MHz with an initial modulation depth of 10%. The frequency of the local oscillator reference was then swept from 10 Hz to 4.5 MHz. The measured normalised spectral response from the MLC output is shown in Fig. 14. The signals with frequency different than the lock-in frequency are rejected. With this light intensity the mixer works close to saturation and therefore due to non-linearities the circuit shows some response to harmonics of the fundamental carrier. Reduction of the modulation depth demonstrated the disappearance of these harmonics and it was found that the system would operate satisfactorily down to modulation depths of 0.5% – a limit set by the measurement accuracy of the equipment and not the pixel itself. Fig. 15 shows a close-up of the 1 MHz fundamental component, illustrating the very narrow response of the lock-in. This method of detecting modulated light offers a high selectivity and makes it possible to recover low signals buried within noise.

Finally, the phase between the incident light and local oscillator was abruptly changed by 180 degrees. The output response of the low-pass filter was observed and Fig. 16 shows this captured output voltage after passing through an off-chip differential to single ended converter (having a gain 10). The output clearly shows that, as expected, the MLC is highly sensitive to the relative phase difference between RF and LO.

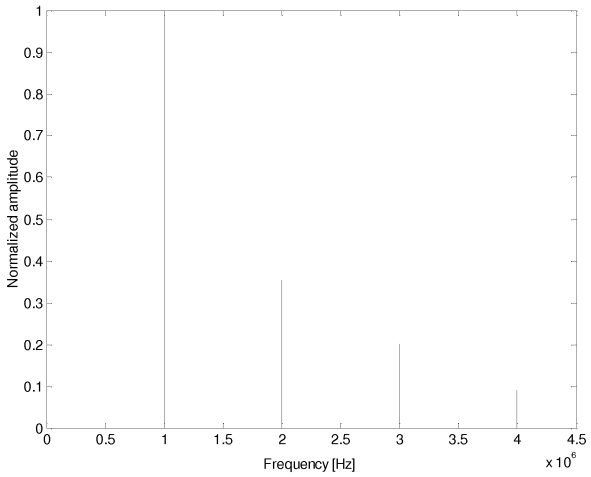

Fig. 14 The low-pass filter output voltage as a function of the local oscillator frequency.

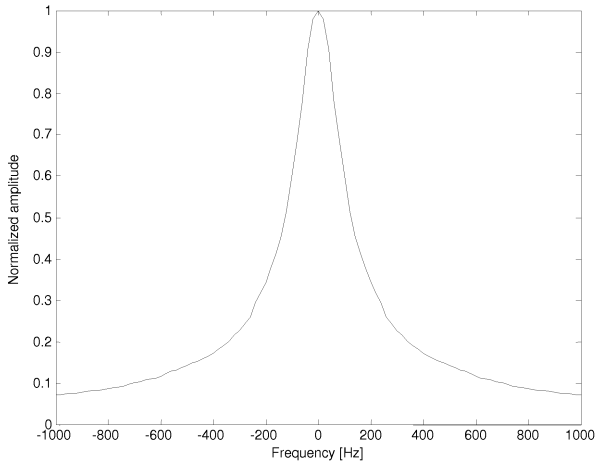

Fig. 15 Close-up of the fundamental 1MHz component from Fig. 14 – centered at 1MHz.

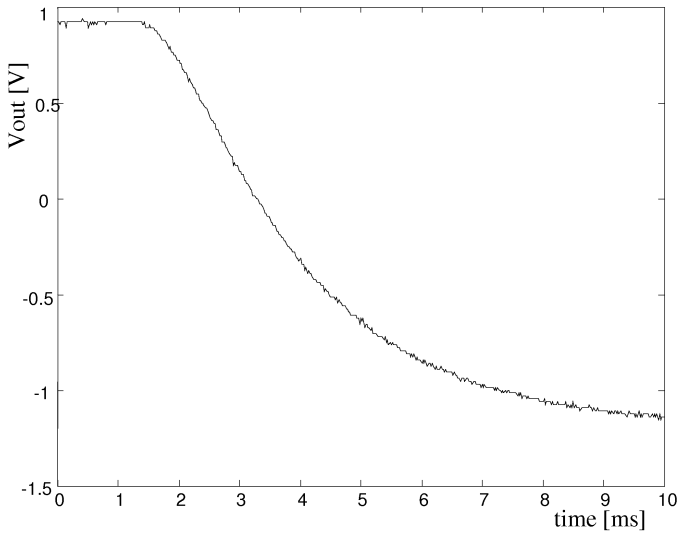

Fig. 16 The output of the 150Hz low-pass filter in response to a 180 degrees phase change between the local oscillator and incoming modulated light.

IV. Conclusion

A lock-in pixel for a CMOS modulated light camera has been presented. This device is capable of detecting modulated light with a modulation depth of 0.5%, with frequencies at 2 MHz and potentially up to 4MHz. The presented pixel is scalable to an array of pixels. It is worth noting that this pixel is not yet optimal and can be made considerably more compact (~100μm x 100μm). The 0.35μm CMOS process is a low voltage, 3.3V process, and as a result the complete pixel draws only 170 μA of current. The experimental results show excellent agreement with simulation results.

Acknowledgment

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